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Growth of InAs and $Bi_{1-x}Sb_x$ Nanowires on Silicon for Nanoelectronics and Topological Qubits by Molecular Beam Epitaxy

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"Happy are the warriors who obtain such an unsolicited opportunity for war which opens the door to heaven. Stand up and perform your duty and, therefore, fight with peace in thy soul."

"A Karma-yogi should fight while treating victory and defeat alike, gain and loss alike, pain and pleasure alike and fighting thus, he does not incur sin"

"You have the right to work, but never to the fruit of work. You should never engage in action for the sake of reward, nor should you long for inaction."

"Perform work in this world, Arjuna, as a man established within himself – without selfish attachments, and alike in success and defeat."

Source (Srimad Bhagavat Gita)

Dedicated to my:

Parents

Brother and Sister

Future Wife !

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List of Acronyms

AC	Alternating Current
BEP	Beam Equivalent Pressure
BJT	Bipolar Junction Transistor
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
DFT	Density Functional Theory
DRAM	Dynamic Random Access Memory
ENG	Equivalent Number of Gates
FET	Field Effect Transistor
FIB	Focused Ion Beam
FTJ	Ferroelectric Tunnel Junction
GMR	Giant Magetoresistance
IC	Integrated Circuit
ITRS	International Technology Roadmap for Semiconductor
LASER	Light Amplification by Stimulated Emission of Radiation
LED	Light Emitting Diode
MAF	Mass Air Flow
MBE	Molecular Beam Epitaxy
MOS	Metal Oxide Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MOVPE	Metal Organic Vapor Phase Epitaxy
MQWs	Multiple Quantum Well
MTJ	Magnetic Tunneling Junction
NVM	Non Volatile Memory

PEC	Photoelectric Cells
PID	Proportional–Integral–Derivative
PRAM	Programmable Random Access Memory
QDs	Quantum Dots
QWs	Quantum Wells
RF	Radio Frequency
S/V	surface-to-volume
SAE	Selective Area Epitaxy
SAED	Selected Area Electron Diffraction
SEM	Scanning Electron Microscopy
SNR	Signal to Noise Ratio
SOI	Spin Orbit Interaction
STT-RAM	Spin Transfer Torque Tunneling Random Access Memory
TCO	Transparent Conductive Oxide
TEM	Transmission Electron Microscopy
TFET	Tunneling Field Effect Transistor
TFNG	Transparent and Flexible Nanogenerator
TI	Topological Insulator
TRS	Time Reversal Symmetry
UHV	Ultra-High Vacuum
UV	Ultra Violet
VLS	Vapor-Solid-Liquid
VS	Vapor-Solid

Chapter 0

General Introduction

In the middle of the 1960s, Gordon Moore, the co-founder of Intel, proposed a law to estimate the evolution of the electronic field: the number of transistors per square inch should double in every two years. The most astonishing point about this prediction is that it remained very accurate for many decades and even drives the nanoelectronics field nowadays. The manufacturing processes progressed from the 50 μm node in the mid 1960s to the 90 nm in 2003, however, the industry faced major bottlenecks to go beyond 90 nm node as short channel effects and quantum mechanical effects araised in the transistors due to miniaturization. In order to address these limitations, the industry focused efforts on material engineering and device architecture. For instance, HfO_2 was adopted to replace the SiO_2 due to its high dielectric constant, the metallic gates were chosen rather than poly-Si gates gates in order to avoid the gate leakage currents and strained silicon was also used in devices to boost the mobility. Furthermore, in 2011, the industry embraced the multi-gate architecture (FinFET) to ensure better gate control over the channel. As it can be seen, the industry worked a lot on new materials to fit the Moore's law up to the 7 nm node (A12 bionic chip from Apple) in 2018.

However, it is unlikely for standard technologies to reach beyond the 5 nm technology node, which led to the concept of Beyond-Moore: a different way of continuing Moore's law beyond scaling limits of current Si technology by either changing material or architecture. In this context, the vertical integration of nanowires on silicon solves some of those fundamental issues. For instance, the vertical integration allows to use nanowires as channel to build 3D Gate-All-Around (GAA) transistors, which is to the date the most optimized configuration. On the other hand, the integration of III-V nanowires on silicon in the last two decades witnessed significant advancements. Hence, its not surprising that, they are regarded as a possible building block for future transistors as reported in the last International Technology Roadmap for Semiconductors (ITRS).

In addition, it is worth mentioning that some key applications need extremely high computational power. The most common example is the modern cryptography which relies on the factorization of very large prime numbers which would be efficiently tackled with new computational approaches based on Qubits and Quantum Computers. The advantages of Qubits is that they rely on a two state quantum mechanical system that can be '0' or '1' or 'both' at the same time con-

trary to standard bits. Because of this property, the quantum computers show exponential gain in processing time with the number of Qubits. For these reasons, the scientific community put high efforts on building Qubits in new materials. In this context, many candidates were studied: Josephson Junctions, spin defined qubits in quantum dots, defects in solids, hyperfine states in ion trapped system system and Majorna Fermions in a semiconductor nanowire hybrid interface. The fundamental requirements for "good" qubits are: long coherence time, insensitive to the external noise and error-free. In this context, Majorana fermions (MFs) can be used to implement topological qubits and can be engineered in a nanowire having Spin Orbit Interactions (SOIs).

In the quest of Mfs, a group from TU Delft led by Prof Leo Kouwenhoven reported the first signatures of Mfs at two ends of a InSb nanowire. In their recipe for building Mfs, the key ingredients are: (i) a nanowire, (ii) high SOIs, (iii) a superconductor and (iv) a magnetic field. Since the nanowire material (InSb) is a semiconductor, the first step is to induce superconductivity by proximity effect. Since the SOIs are large in InSb, the external magnetic field allows the creation of topologically protected states at the superconductor/semiconductor interface; and MFs can appear as zero energy modes. From the material point of view, replacing the InSb nanowires by new nanoscale 3D Topological Insulators (3DTIs) could be interesting. Indeed, 3DTIs are a new family of materials that are conducting at their surface and isolating in the core. They were first theoretically predicted a decade ago in 2007 by Fu and Kane from University of Pennsylvania, and measured experimentally one year later by a group of scientists led by Prof. Zahid Hasan from Princeton University.

In the context of high electrons mobility transistors and topological qubits, this thesis aims at developing new materials that are suitable for these applications. The materials we developed are nanowires based on InAs and $Bi_{1-x}Sb$. The high mobility of InAs is interesting for nanoelectronics and similarly the 3D topological behavior of $Bi_{1-x}Sb_x$ can be used in the realization of Mfs based Qubit devices. In both cases, the primary objective is to improve the quality of the nanoscale materials while addressing some of the key technological bottlenecks. In this thesis work, we study and demonstrate full CMOS compatible InAs nanowire integration on Si by Molecular Beam Epitaxy (MBE), and the growth of $Bi_{1-x}Sb_x$ nanowires on Si with controlled composition.

The architecture of the thesis is the following:

The Chapter 1 presents the nanowire research field from the materials to the applications. First, a few key historical moments are reported briefly and followed by a discussion on different possible geometries that emerged along with the progress in nanowires growth. Finally, 10 key applications are proposed and for each of them the advantages of the nanowire geometry are listed.

The Chapter 2 presents the tools and technologies we used for nanowire growth, characterization and the analysis method. The chapter starts with a brief description of a standard Molecular Beam Epitaxy (MBE) system followed with a brief introduction to Scanning Electron Mircrosopy (SEM) and Transmission Electron Microscopy(TEM). Similarly, the X-Ray Diffraction (XRD) measurement is discussed briefly. At the end, the image processing steps and the data treatment procedures, that were developed using standard open source tools are presented. This semi-automatic image processing and fully automatic data analysis facilitated the statistical analysis of nanowires especially in chapter 4.

The Chapter 3 provides an overview of the nanowire growth and the nucleation processes. First the Vapor-Liquid-Solid (VLS) growth mechanism and the thermodynamic and kinetic aspects during nucleation are discussed. Next, the Vapor-Solid (VS) growth mechanism is presented, as well as, the two possible crystalline structures: Zinc Blende (ZB) and Wurzite (WZ). Finally, the Density Function Theory (DFT) is briefly explained.

The Chapter 4 deals with the integration of InAs nanowires on Silicon for high mobility nanoelectronics. In this chapter, first a brief introduction of the electronics technologies is presented. This includes a historical description, the scaling laws, the issues with the 90 node technology and the necessity of new nanoscale materials. Next , the state of the art is presented before we focus on our contribution where we report first the advantage of an hydrogen treatment. Next, a full CMOS compatible process that even addresses the Back-End-of-Line (BEOL) thermal limit is presented leading to fully CMOS compatible InAs nanowires on silicon. In the later part, a full growth study on patterns in Silicon is presented leading to the integration of InAs and InAsSb nanowires. The chapter also enlightens a change in the growth mode from VS to VLS. Finally DFT simulations are developed to qualitatively characterize the surface treatment.

The Chapter 5 deals with the integration of $Bi_{1-x}Sb_x$ nanowires on Si with a controlled Sb composition. The chapter starts with the brief introduction to quantum computing, to the material aspects of quantum computing and to the topological qubits. Following, 3D topological materials are presented, before we report our contribution to the field. First the initial growths of $Bi_{1-x}Sb_x$ nanowires are presented, allowing good control of the Sb. In parallel, a full investigation of the influence of Bi, Sb and the growth temperature is presented, leading to different nanoscale geometries. In addition, a complete TEM characterization of the $Bi_{1-x}Sb_x$ nanowires is carried out showing defect free single crystalline nanostructures having 3 kind of facets. Finally EDS-TEM and XRD compositions are compared showing good agreements, and low Sb composition compatible with the TI region are achieved.

Chapter 1

Nanowires and Applications

The history of nanowires dates back to 1964 when Wagner and Ellis from the Bell Telephone Laboratory used the Vapor-Liquid-Solid (VLS) mechanism to grow single crystalline Si nanowhiskers[1]. It was however only in the mid-1990s that the group of Prof. K. Hiruma, from Hitachi in Japan, synthesized the first III-V nano whiskers[2–4] including a PN junction[5]. Thanks to the reduction of their diameter in the following years, they were finally renamed "nanowires". At the beginning of the 21st century, and due to their unique geometry, nanowires gathered an immense research interest and are at present one of the most explored topic. The bar plot in 1.1 repensents the evolution of the field since 2000 and further highlights the attentions that nanowires received recently.

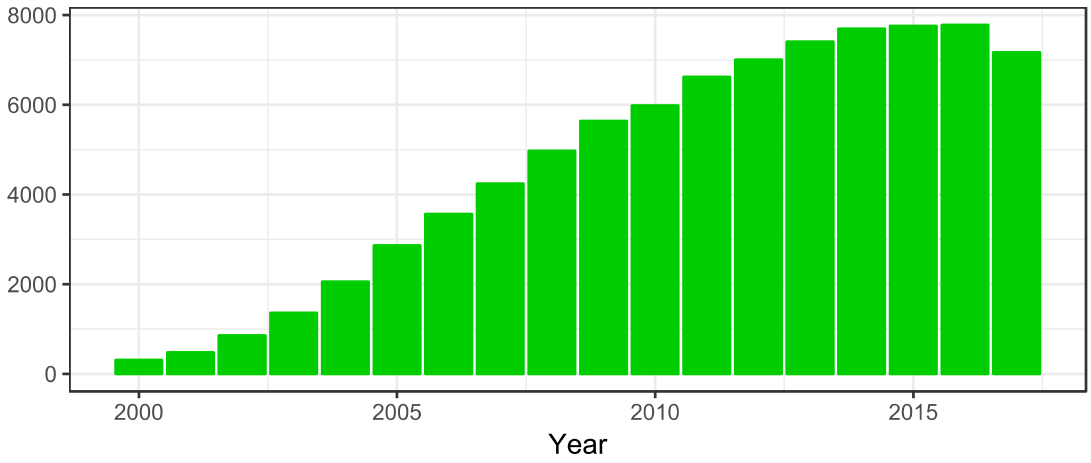


Figure 1.1 – *Number of Publications recorded with the keyword "nanowires" (y-axis) since 2000 for each years (x-axis) . Source: Web of Science (http://apps.webofknowledge.com/)*

Nanowires are 1D nanostructures, whose diameter is measured in few tens of nanometers(nm) and length in few microns(μm). Consequently, their surface-to-volume ratio (S/V) is high compared to their 2D counterparts. Additionally, this 1D geometry can withstand high strain and fabrication of defect free structures with high crystalline quality is possible. Thus, one can engineer the materials' intrinsic properties at nanoscale including electrical, optical and magnetic properties; making them ideal candidates for the development of new nanoscale devices in the fields of nanoelectronics,

optoelectronics, memories, energy etc. Furthermore, since the nanowire diameter can be smaller than the Bohr radius, quantum mechanical properties start to become prominent, which makes them ideal experimental tools for exploring the quantum world. Finally, the large number of options that are available to synthesis nanowires (see figure 1.2), explain why this field has become the frontier of numerous multidisciplinary research themes.

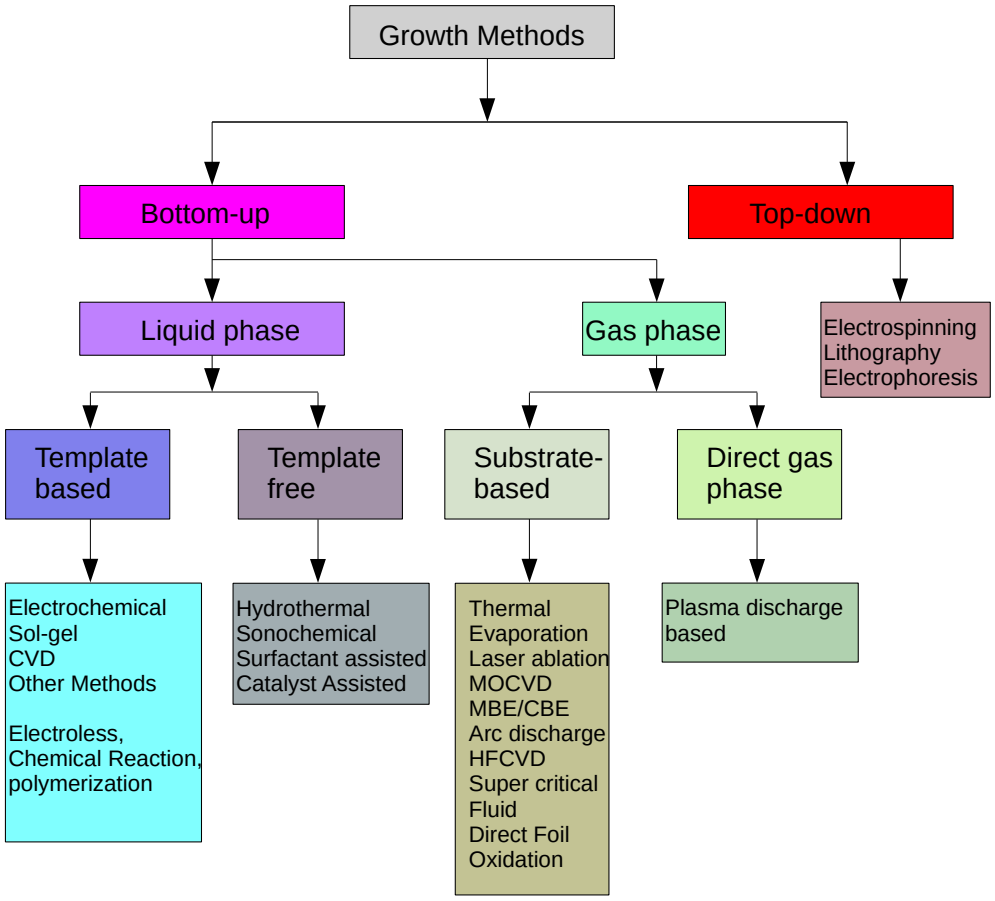


Figure 1.2 – *Different synthesis methods reported for nanowires growth. (Adapted from Mayyappan[6])*

Thanks to the development of new synthesis processes (figure 1.2), and advances in the control of conventional epitaxial tools, including Molecular Beam Epitaxy (MBE) and Metal Organic Vapor Phase Epitaxy (MOVPE); new nanostructures were developped such as axial or lateral heterostructures[7] [figure 1.3 (b and c)] and superlattices[8] [figure 1.3 (d and e)]. The possibility of combining materials with large lattice mismatches opened new opportunities for bandgap engineering; and the precise control of the catalyst shape and composition allowed to develop new nanoscale geometries (figure 1.3) including branched[9] and kinked[10] nanowires [figure 1.3(g)], nanoflakes[11] [figure 1.3(i)], nanoribbons[12] [figure 1.3(h)] and nanotrees[13] [figure 1.3(f)]. Taking advantage of this new nanoscale "zoology", several devices are now developped such as Tunneling Field Effect Transistors (TFET) using a flake or a ribbon as a channel[14] or efficient hydrogen generators using the nanotrees geometry to improve the surface to volume ratio[15].

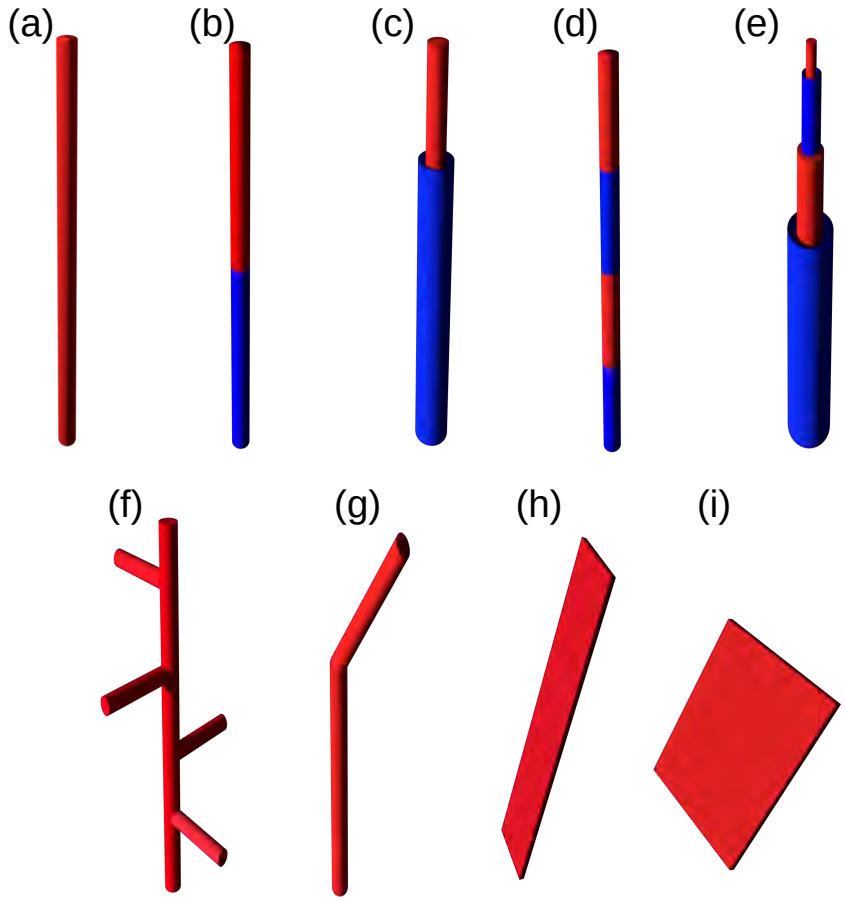


Figure 1.3 – *Nanowire and beyond nanowire structures.(a) nanowire, (b) axial nanowire heterostructure, (c) core-shell heterostructure, (d) axial nanowire superlattice, (e) lateral core-shell superlattice, (f) nanotree, (g) kinked nanowire, (h) nanoribbon and (i) nanoflake*

The nanowire studies generally focus on growth, characterization, device fabrication and modeling. The commonly used materials are : III-Vs, IVs, II-Vs, sulphides, oxides, nitrides, chalcogenides, carbides, silicides etc. Based on their intrinsic properties, their geometry, the functionnalization of the surfaces or their crystalline structure, several fields of application can be adressed, as presented in the following:

1. Nanoelectronics
2. Spintronics
3. Phase Change Memories
4. Piezoelectrics
5. Optoelectronics
6. Solar Cells
7. Water Splitting and H_2 Generation
8. Thermoelectrics
9. Li-Ion Battery
10. Sensors

1.1 Nanoelectronics

The invention of the transistor is one of the big achievement of the 20th century. It is a 3 terminal switch where the flow of current between two terminals is controlled by a third one. The transistor is the fundamental building brick of each processor that is the core of the Central Processing Units (CPUs). In the framework of Moore's law, nanoelectronics can nowadays be divided in three: More Moore, More-than-Moore and beyond CMOS. More Moore is in compliance with the Moore's law and is basically following the trivial trends onscaling and packaging densities. More-than-Moore is incorporating additional functionalities such as sensors, RF blocks, etc. to the current CMOS technology. Beyond CMOS starts where the current scaling laws fail, because of the quantum mechanical effects that arise, and where the new CMOS compatible technologies step up. The possible candidates proposed in the International Technology Roadmap for Semiconductors (ITRS)[16] are: the semiconducting nanowires (figure 1.4), the carbon nanotubes, the graphene, and the single electron transistors.[17] The advantages of the nanowire integration are: (i) the vertical integration of nanowires is promising for the aggressive transistor down-scaling, (ii) small diameters allow a good electrostatic control of the transistor channel and (iii) the heterostructure engineering allows the realization of Tunnel FETs.

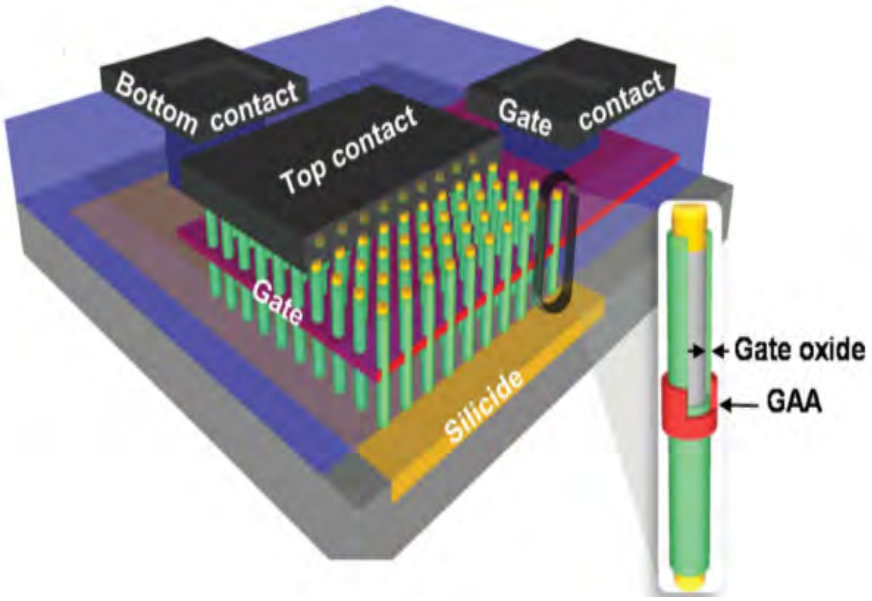


Figure 1.4 – *Sketch of a vertical nanowire array based field effect transistor. (Larrieu et al.[18])*

The 4th chapter of this thesis is focused on nanoelectronics and on the vertical integration of bottom-up InAs nanowires on silicon with a CMOS compatibility. Similarly, the chapter 5 is centered on another beyond CMOS option: the development of topological qubits based on $Bi_{1-x}Sb_x$ nanowires for quantum computing.

1.2 Spintronics

Spintronics refers to the generation, manipulation, transport and detection of spin-polarized current utilizing two of the electron properties: the spin and the charge. It bridges the gap between charge based computers and magnetic memories. Spintronics devices can be either active or passive. Active devices include spin valves, Giant Magetoresistances (GMR)[19], Magnetic Tunneling Junctions (MTJ)[20], Ferroelectric Tunnel Junctions (FTJ)[21] and Spin Transfer Torque Tunneling Random Access Memories (STT-RAM)[22]. Similarly, passive devices are spin FETs[23] and 2i/p NAND gates[24]. The advantages of nanowires for spintronic devices are: (i) a wide range of material can be developed, (ii) the necessity of lower external magnetic field compared to bulk, (iii) an easy magnetization along the nanowire axis and (iv) an ideal platform for magnetic domain walls because of the two fold degeneracy that the nanowire structure provides.

For example, a spin valve consists of 2 magnetic layers, a hard one called “fixed” layer and a soft one called “free” layer, that are separated by a non-magnetic spacer. Depending of the relative magnetic alignment between the hard and the soft layers, the electrical resistance of the device changes. Using nanowires for the soft magnetic layer would thus be advantageous since the external magnetic field could be decreased. The most used material for these applications is silicon[25,26]. Otherwise, core-shell geometries can also be advantageous for spin valve applications by combining in the same nanowire the “free” and the “fixed” layers (figure 1.5).

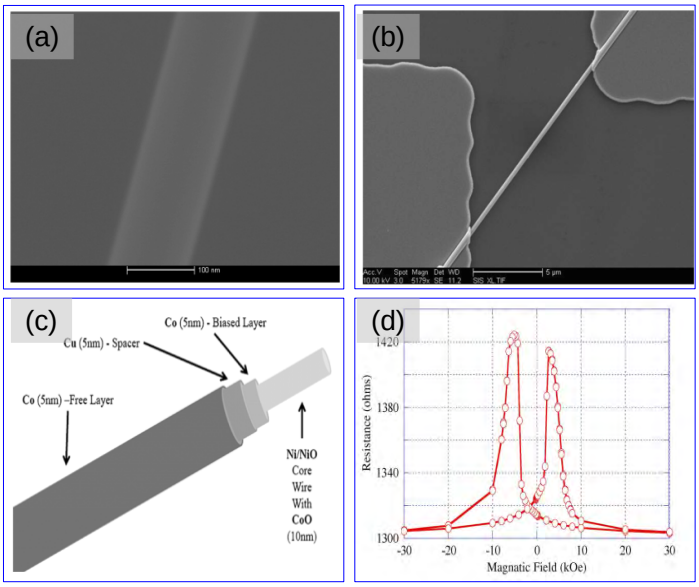


Figure 1.5 – *Nanowire based spin-valve. (a) Close up scanning electron microscope image of a typical Ni/NiO nanowire. (b) Scanning electron microscope image of an isolated nanowire spin valve on an insulating substrate with 150 nm thick Ta contacts for magnetoresistance measurements. (c) Schematic of the implemented spin valve multilayer on a nanowire core. The first CoO shell biases the Co reference layer. A Cu spacing layer is then followed by the Co reference layer. (d) Magnetoresistive response of a nanowire spin valve at 10 K following a 30-kOe field cool at 380 K. The magnetoresistance value is approximately 9%. (Chan et al.[27])*

1.3 Phase Change Memories

A Phase Change Memory (PCM), also known as Programmable Random Access Memory (PRAM), is a form of Non Volatile Memory (NVM), which offers a high density storage at low cost. It is easily upscalable and has a speed close to the Dynamic Random Access Memory (DRAM) as shown in table 1.1. Moreover, PCM enables writing information without erasing it before, and its durability of 10 million write cycles is extremely high compared to the 3000 cycles of a flash one. It has consequently emerged as a very strong candidate for the next generation of solid state NVM. This technology is based on the large difference in resistivity of a low ordered amorphous phase and a highly ordered crystalline one. The crystalline phase (low resistance) can be transformed into an amorphous one (high resistance) and vise versa when probed with electric/laser pulses; resulting in SET (low resistance) and RESET (high resistance). The major advantages of the nanowire geometry are: (i) a better retention time compared to the conventional devices, (ii) fewer defects, (iii) better surface properties, (iv) a lower power consumption during SET/RESET operations and (v) it fits the aggressive scaling standards of CMOS.[28]

Attributes	PRAM	EEPROM	NOR	NAND	DRAM
Non-Volatile	Yes	Yes	Yes	Yes	No
Scalability	<10 nm	~ 4x nm	~ 3x nm	~ 1x nm	~ 2x nm
Bit Alterable	Yes	Yes	No	No	Yes
Erase Required	No	No	Yes	Yes	No
Software	Easy	Easy	Moderate	Hard	Easy
Write Speed	~ 100 MB/s	~ 30 MB/s	~ 1 MB/s	~ 20 MB/s	~ 1GB/s
Read Speed	50 - 100 ns	~ 200 ns	70 - 100 ns	15 - 50 µs	20 - 80 ns
Endurance	$10^{6\text{-}8}$	$10^{5\text{-}6}$	10^{5}	$10^{4\text{-}5}$	Unlimited

Table 1.1 – *Comparison of Different Memories*

All the phase change materials, except In_2Se_3[29], are chalcogenides as their thermal conductivity is extremely low in the crystalline phase[30]. It is worth noting that chalcogenide alloys were commonly used in optical memory devices such as: Compact Disc (CD)[31], Digital Versatile Disc (DVD)[32] and blue ray technologies[33]. While the DVD is based on $Ge_2Sb_2Te_5$ material[32] (there is 30% difference in reflectivity between the amorphous and the crystalline phase), blue ray[33] technology uses Ag-In-Sb-Te (AIST) materials. The industrial success of these chacogenide based storage medium inspired the concept a non volatile memory of high durability with a speed close to DRAM, which is commonly referred as universal memory[34].

In literature, the bottom-up integration of GeTe[35,36], $Ge_2Sb_2Te_5$[37,38], Sb_2Te_3[35,39], In_2Se_3[40] nanowires is demonstrated using the VLS mechanism and a MOVPE growth system. Among these materials, $Ge_2Sb_2Te_5$[37,38] gathered significant interests because of its lower thermal conductivity that enables fast switching speed with low power consumption. A major breakthrough was reported by Jung et al.[41], who managed to switch a crystalline nanowire into an amorphous one with a very low current and demonstrated the threshold switching between the two phases using an electric field[42]. The authors further revealed a significant improvement in power consumption employing thinner

$Ge_2Sb_2Te_5$ nanowires. In another paper[42], the same group developed a 3 level switch, using a core-shell geometry with a 50nm thick GeTe shell and a 100nm $Ge_2Sb_2Te_5$ core. In this heterostructure, the core switches to an amorphous state at 1.3 mA, whereas the shell becomes amorphous at 1.6 mA. This highlights a concept beyond the present binary logic system with a 3^N level of data storage[42], which further extends up to 10^N levels for "beyond von-Neumann" computing.

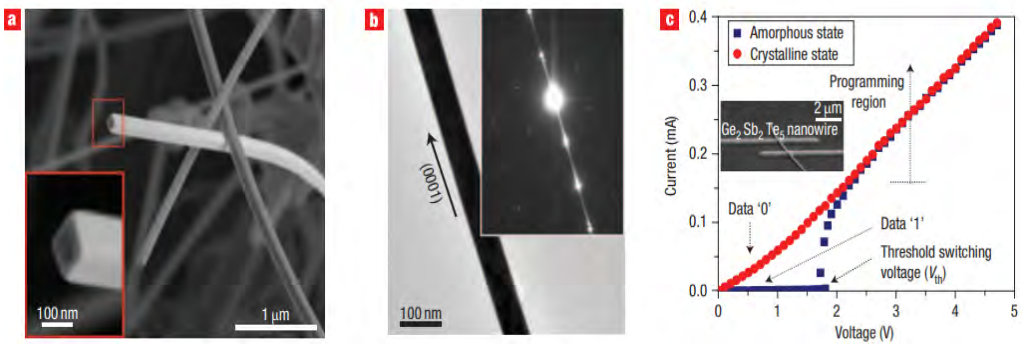


Figure 1.6 – *Phase Change Memory with GeSbTe nanowires. (a) SEM image , (b) TEM image and (c) electrical characterisation (Lee. et al.[38])*

1.4 Piezoelectrics

The piezoelectricity is the faculty of some materials to transform a mechanical strain into an electric current by exploiting the charge imbalance in the structure and vice versa. The first report of a piezoelectric device using nanowires was published by Wang and Song[43] in 2006. Thanks to their mechanical properties, nanowires are thus ideal candidates for creating nanoscale self powered active sensors for monitoring applications such as: weight measurement, skin deformation, tyre pressure, etc[44]. Two configurations are then possible for the device: either using a lateral bending or a vertical compression[45].

If the strain is applied laterally at the top of the nanowire, an asymmetric potential is initially generated due to the stretch (+ve) and compression (-ve) of the inner and outer side of the nanowire. This changes the piezoelectric potential profile along the nanowire. If an ohmic contact is taken at the grounded side and a Schottky one on the other side, electrons can flow from the grounded electrode to the external circuit and finally to the other side of the nanowire, where the Schottky prevents shortcuts. When the strain is released, the potential drops back to zero[44] . On another hand, if a compressive strain is applied vertically to the device [see figure1.7 (d)], higher output currents can be achieved. In this case, vertical nanowires are connected to two Schottky electrodes. When these nanowires are compressed, a piezoelectric potential is developed across the nanowire axis. The conduction band and the Fermi level are then lifted. Since there is a Schottky barrier at both ends, it forbids electrons to pass though the nanowire-electrode interface. As a consequence, electrons flow through the external circuit on the counter electrode generating positive electric pulses. When com-

pression is released, the piezoelectric potential vanishes and the equilibrium state inducing energy difference on the opposite direction is broken, which leads to a negative electric impulse. Hence, the overall process output is an alternative current (AC)[44].

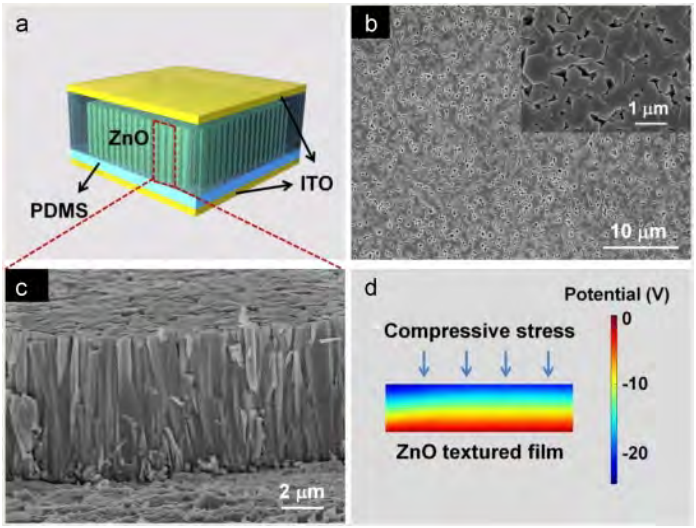


Figure 1.7 – *Nanowire based piezoelectric devices (a) 3D schematic of a transparent nanogenerator using a ZnO nanowire array (b) Top-view SEM image of the as-grown ZnO NW array. (c) Cross-sectional SEM image of the as-grown ZnO nanowire array and (d) demonstration of the working principle of a Transparent and Flexible Nanogenerator (TFNG) from the numerical calculations of the ZnO piezopotential. (Lin et al.[46])*

Moreover, Wurtzite based III-V and II-VI nanowires gathered significant attention since the lack of symmetry centers in Wurtzite crystals leads to a greater piezoelectric effect. Indeed, due to this crystalline structure, the relative displacement of cations and anions in the crystal facilitates the conversion of mechanical strain into an electrical potential and vice versa. The considered nanowires are: ZnO[47–49], GaN[50–52], InN[53], CdS[54] and CdSe[55]. In this list, the most investigated one is ZnO, but 1V output can also be obtained using GaN and InN nanowires of high crystalline quality[44].

In addition to new material synthesis, researches also focus on device fabrication and process optimization. For example, Xudong et al.[56] implemented zigzag electrodes on top of vertically aligned nanowires and observed an enhancement of the conductivity without the need of any external Schottky contact. Additionally, this zig-zag design supports a wide range of frequencies, ranging from Hz to MHz, that is adaptive to a wide range of applications. Similarly, Xu et al.[57] built a 3D nanogenerator using vertical ZnO nanowires, which provides a high control over the packaging by eliminating the height restrictions. Finally, Choi et al.[58] revealed the uniformity of the potential distribution for nanowires embedded in PMMA, which gives high power output (6-10 times higher than without PMMA) and enhances the mesoscopic behaviour[58,59]. Using PDMS instead of PMMA, Lin et al.[46] fabricated transparent and flexible nanogenerator and Zhu et al.[60] demonstrated an output power reaching 58V.

1.5 Optoelectronics

Optoelectronics applications are based on light/material interactions. The three main applications using nanowires are: photodetectors, Light Emitting Diode (LED) and Light Amplification by Simulated Emission Reaction (LASER) (see figure 1.8). The benefits of using semiconducting nanowires are: (i) a wide coverage of the solar spectrum using proper materials, (ii) an efficient band-gap engineering is possible, which provides another degree of control on the absorption and emission of light, (iii) new crystalline structures with new bandgaps are possible (Wurtzite) (iv) less divergence and high carrier confinement for light emitting applications, and (v) high sensitivity and high Signal to Noise Ratio (SNR) for light detectors.

In the literature, Si[61] and n-type CdS[62] based nanowires photodetectors are the most studied ones for detection in the visible range. In addition to standard p-i-n junctions that can be implemented in Si[63], a major advancement was the fabrication of an avalanche photodiode using a p-doped Si / n-doped CdS herojunction in a single nanowire[64]. Moreover, other low bandgap materials were investigated for light detection in the visible range such as CdSe[65], ZnSe[66], CdTe[67] and ZnTe[68]. In the case of the Visible / Ultra Violet (UV) region, a strong selectivity was reported using both GaN[69] and ZnO[70] nanowires, but other materials such as Ga_2O_3[71] and In_2O_3[72] are still considered. In addition, using core-shell heterostructures, the material bandgap can be tuned precisely for optimizing the device performances as reported for InGaN/GaN[73], GaAs/AlGaAs[74], InGaP/GaAs[75] and GaAs/InGaP/GaAs[76].

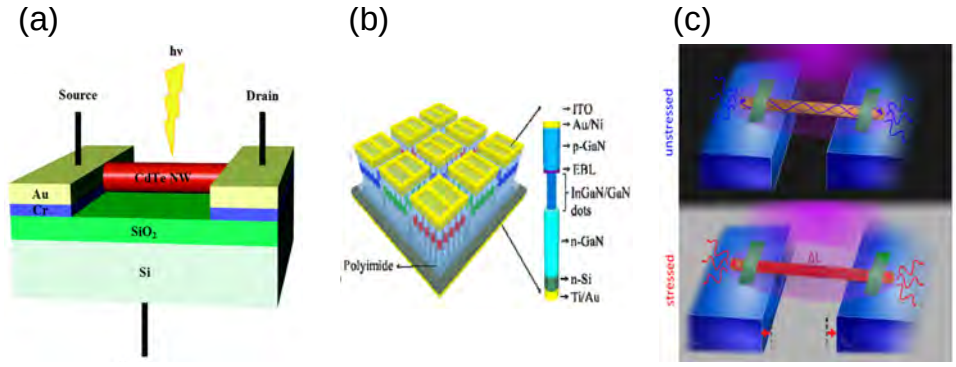


Figure 1.8 – *Nanowires based optoelectronics (a) photodetector (b) LED and (c) Laser. (Image sources: (a) Shaygan et al.,[67] (b) Wang et al.[77] , and (c) Zapf et al.[78]))*

Now, if we consider LED applications, one must mention two recent highlights: (i) the 2014 noble prize of Physics was awarded to Isamu Akasaki, Hiroshi Amano and Shuji Nakamura "for the invention of efficient blue light-emitting diodes which has enabled bright and energy-saving white light sources" (*https://www.nobelprize.org/*) and (ii) a few LED manufacturing companies such as Aledia (https://www.aledia.com/en/) and Glo (http://www.glo.se/) are developing nanowire based LEDs. If historically, Haraguchi et al.[5]demonstrated the world's first nanowire based LED using GaAs nanowires for emission in the near infrared; Nitride-based nanowires (AlN, GaN and InN) are better candidates for industrialization since their bandgap (1.8-3 ev) fits the visible spectrum[77]. In these devices, the core-shell heterostructure is optimized by growing a n-type core and a p-type

multi-shell with Multiple Quantum Well (MQWs) based on GaN/InGaN[79] materials. Each of the primary colors is then optimized giving for instance a 60% efficiency for blue and 40% efficiency for green. Red Green Blue (RGB) or Red Yellow Green Blue (RYGB) lights are finally combined to obtain the desired color.

In the case of UV laser, ZnO is the most explored material because its exciton binding energy is larger than the thermal energy, which enables exciton recombinations even at room temperature and thus facilitates stimulated emission at lower threshold. The first room temperature ZnO nanowire laser was reported by Huang et al.[80] in 2001.

1.6 Solar Cells

A solar cell, or photovoltaic cell, is an electrical device that converts the energy of light directly into electricity thanks to the photovoltaic effect, which is a physical and chemical phenomenon[81]. The building brick of a solar cell is a PN diode, which working principle is same as a normal one. Photons, that have an energy hv (h being the planks energy constant and v the momentum of photon) higher than the gap, create electron-hole pairs that are spatially separated in the nanowire thanks to a p-n junction. The current (I) is generated once electrons and holes are collected at the top and bottom electrodes. Due to their small dimensions, nanowires can be advantageous for solar cell applications since they allow: (i) enhanced charge collection and transport due to an increased surface area, (ii) core-shell junctions, with absorption along the nanowire axis, in which minority charge carriers travel radially, reducing possible recombinations, (iii) the in-plane light-trapping, thanks to the scattering and optical modes that arise from nanowire arrays and (iv) to increase the shunt resistance and reduce the series resistance. Moreover, it was theoretically demonstrated[82,83], that if the diameter and the pitch of a nanowire arrays are optimized, the light absorption can be equivalent to 2D technologies, but using 10 % of the total materials.

From the industrial point of view, silicon is the most commonly used material. The maximum efficiency for a silicon single junction cells, is about 27.6% for crystalline Si cell[84], and about 46% for a multi junction cell[84]; but increasing the efficiency remains a key issue. The record efficiency, that is demonstrated for thin film solar cells, is about 27.6 % for Si while it is 24.2 %[85] for InP, 29.3 %[84] for GaAs and 22.9 %[84] for CdTe. Up to the date, the highest recorded efficiency is to the date is 46.0 % from multijunction heterostrucuture[84,85]. When compared to the solar light spectrum (with an energy maximum around 1.5eV), InP -1.27 eV,[86,87] GaAs-1.43 eV[87] and CdTe-1.44 eV[88] have higher conversion efficiencies than Si –1.11 eV. This explains why the growth of InP and GaAs nanowires is of prime importance for the development of nanowire based solar cells, and is studied on different substrates such as Si[89], glass[90], glass with Transparent Conductive Oxide (TCO) coating[91] etc. The record efficiency for a nanowire solar cell is 13.8 % (figure 1.9) using InP nanowires with p-i-n junctions[92]. In the case of GaAs, and due to the high recombination rate on lateral facets, core-shell GaAs/AlGaAs heterostructures are used in order to passivate surfaces and improve carrier lifetimes[93].

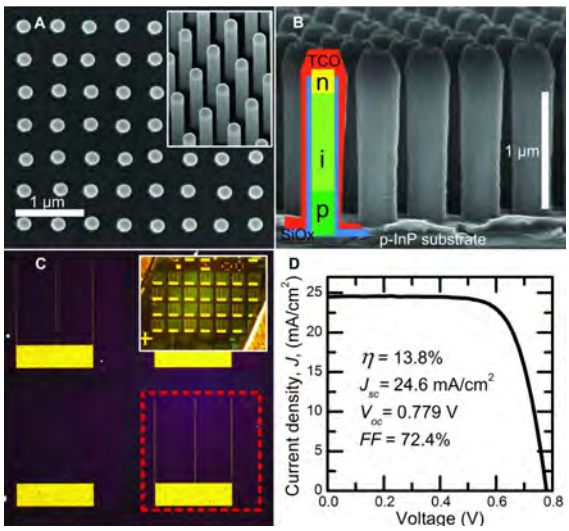


Figure 1.9 – *Nanowire based solar cell. Characterization of NW-array solar cells: (A) Top-view Scanning Electron Microscopy (SEM) image of a nanowire array (B) Side-view SEM image of the NW solar cell. (C) Optical microscope image of nanowire solar cells. (D) I-V curve (Wallentin et al.[92])*

1.7 Water Splitting and H_2 Generation

H_2 generation, also known as artificial photosynthesis, is another aspect of the photovoltaic process. It allows to convert the solar energy into hydrogen (H_2) thanks to a Photo Electric Cells (PEC) using the process of water splitting[94,95] . In order to be commercially interesting, an efficiency of at least 5% is necessary. The charge generation process is same than described in the solar cell section (1.6), but the charge collection occurs at the semiconductor/electrolyte hetero-junction interface. The minority carriers react at the surface, while majority carriers travel through the bulk in order to perform complementary reactions at the counter electrode. Hydrogen is produced at the cathode and Oxygen at the anode. The nanowire advantages for this application are: (i) an enhanced light trapping and charge collections, (ii) an enhancement of the redox reaction rate, (iii) and it facilitates the architectural "Z-scheme"[96,97], a concept using two light absorbers, which allows the larger absorption of the solar spectrum and thus larger voltages.

The electrochemical potential of water is 1V, which determines the choice of materials. The series of different chemical reactions that occurs during this process is listed below[98]:

$$H_2O \longrightarrow H_2 + \frac{1}{2}O_2 \qquad \Delta E = 1.23V$$

$$CO_2 + H_2O \longrightarrow HCOOH + \frac{1}{2}O_2 \qquad \Delta E = 1.4V$$

$$CO_2 + H_2O \longrightarrow HCHO + O_2 \qquad \Delta E = 1.34V$$

$$CO_2 + 2H_2O \longrightarrow CH_3OH + \frac{3}{2}O_2 \quad \Delta E = 1.21V$$

$$CO_2 + 2H_2O \longrightarrow CH_4 + 2O_2 \quad \Delta E = 1.06V$$

Different materials have been studied, including semiconducting nanowires, for both the photo-anode and the photo-cathode. The most promising candidates for photo-cathode are Si[99,100] and InP[101] nanowires since they should yield to high current density and high photovoltages. On the other hand, the oxide and III-V based nanowires, including TiO_2[99], n-Fe_2O_3[102], ZnO[103], GaN[104,105], GaP[106], InGaP[107], InGaN[107], and GaAs[108] have been used for the photo-anode. The biggest issues, that need to be overcome, are the protection of the electrode surface and the increasing of the redox surface area[109].

In order to address these issues, significant research efforts have been devoted to the surface engineering. For Instance, heterostructures such as WO_3/Fe_20_3[110] , Fe_20_3/In_2O_3[111] and $Fe_20_3/MgFe_2O_4$[112] increase the absorption range, promote charge transfer, and improve the interface electric field. It is also possible to protect surfaces with a coating layer in order to improve the stability: for example a TiO_2 layer over Cu_2O nanowires[113]. Similarly, it is possible to improve the electrode stability by decorating Cu_2O nanowires with Pt nanoparticles[114], or depositing CoBi[115]and CoPi[116]on $BiVo_4$ nanowires. Recently, the nanotree geometry became extremely popular since it increases the surface to volume ratio. Finally, Liu et al[98]developed a fully integrated nanosystem (figure 1.10), using a nanotrees geometry with Si as trunk (photo-cathode) and TiO_2 as branches (photo-anode).

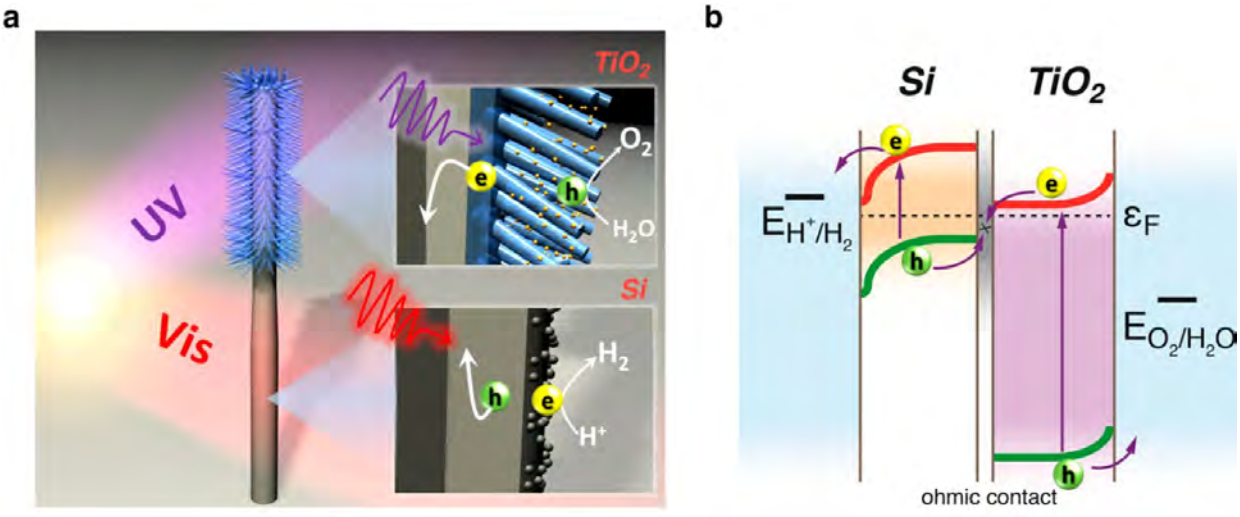


Figure 1.10 – *Nanowire based water splitting device. (a) 3D schematic of a nanotree based system and (b) the corresponding band diagram. (Liu et al.[98])*

1.8 Li-Ion Battery

Sony introduced Li-ion battery for the first time back in 1991 and its demand swore up with the boom of the consumer electronics devices especially mobile phones and laptops. This technology, whose key features are: low cost, longer life span, high current density and good reversibility, remains one of the most active research domain as continuous efforts on improving the technology are crucial for new applications such as hybrid and electric cars. The US Department of energy points out three key requirements in order to establish a consumer market for electrical vehicle using this technology: (i) we should improve the density from 100 $WhKg^{-1}$ to 150 $WhKg^{-1}$, (ii) it should withstand at least 1000 charge cycles, and (iii) the price should be decreased by two third[117].

As shown in figure 1.11, a Li-ion battery is composed of three major components: the anode, the cathode and an the electrolyte in between. When charging the battery, a Li+ ion from the cathode (mostly LiCoO) passes through the porous and conducting electrolyte towards the anode (mostly graphite). Once it reaches the anode, an intercalcination reaction takes place. The opposite phenomenon is observed during discharge. In this context, the nanowire geometry is attractive for creating low cost and high density electrodes: (i) it allows direct pathways for ions, (ii) the high surface area reduces the charge and discharge time, (iii) the mechanical stability accommodates the volume expansion allowing thus a better lifespan, and (iv) complex architectures are possible with nanowires. Figure 1.11 shows a Li ion battery made of three nanowire modules, which further illustrates these advantages[118] .

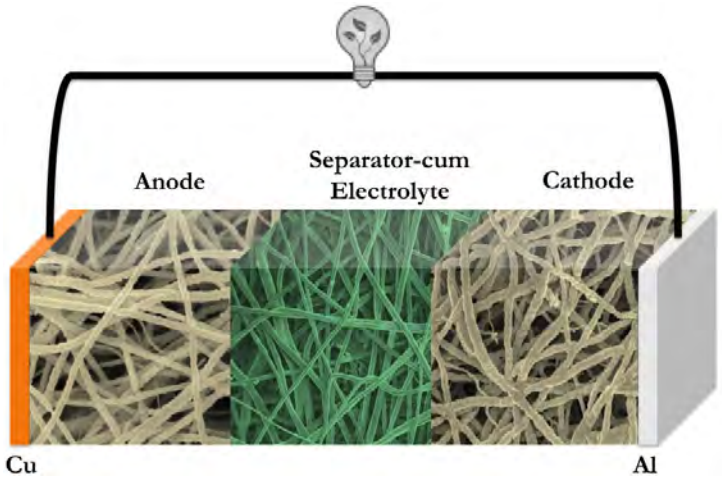


Figure 1.11 – *Nanowire based Li-ion battery. (Arvindan et al.[118])*

A large set of materials has been investigated for both the anode and the cathode. For the anode, the list includes nanowires made of Si[119–121], Ge[122], SnO_2[123], ZnO[124], CuO[125], Co_3O_4[126], MnO_2[127], Fe_3O_4[128] etc. Similarly, the oxide based intercalcination materials for the cathode are $LiCoO_2$[129], $LiFePO_4$[130] and $LiMn_2O_4$[131] nanowires. The high crystalline quality of these oxide based nanowires enhances the charge and discharge rates with small changes in volume. The mostly used material for the anode is Si, thanks to the high capacity of the Si/SiO_2 interface (10 times of the graphite), but the very high expansion coefficient (300%) of Si nanowires during lithiation makes them fragile

and reduces the total number of possible cycles[132]. As a result, a large number of studies have been focused on either reducing the volume expansion of these nanowires by coating them[133,134] or on developing new structures such as porous one[135], nanofibres[136] and heterostructures[137,138].

1.9 Thermoelectrics

The thermoelectric effect is the direct conversion of temperature differences to electric voltage and vice versa via a thermocouple. “A thermoelectric device creates voltage when there is a different temperature on each side. Conversely, when a voltage is applied to it, it creates a temperature difference”[139]. The term "thermoelectric effect" encompasses two separately identified effects: the Seebeck and the Peltier effect. The Seebeck effect describes the electrical voltage generated from the temperature gradient and thermoelectric generators are based on this principle. The Peltier effect describes the heating or cooling at an electrified junction of two different conductors and thus is implemented in the thermoelectric coolers. The advantage of nanowires is that they provide a perfect platform for improving the themoelectric figure of merit (ZT) by limiting the phonon diffusion along the wires while keeping a good electrical conductivity. At present, the standard value of ZT is 1[140], which, if increased to 3, should multiply by 10 the number of possible applications[140]. Figure 1.12 presents the schematic of a nanowire based thermoelectric generator, where fully vertical Si nanowire arrays are placed between hot and cold electrodes.[141]

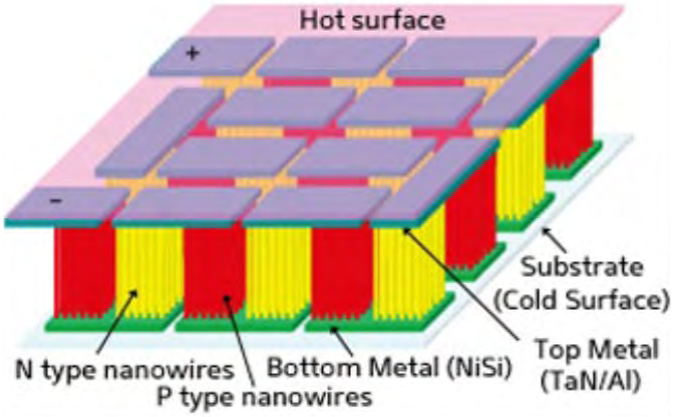


Figure 1.12 – *Nanowire based thermoelectric generator. P and N types Si nanowires arrays are placed between hot and cold surfaces via metallic contacts. (Li et al.[141])*

Mathematically, the Seebeck effect can be described as:

$$S = -\frac{\Delta V}{\Delta T} \tag{1.1}$$

where S is the Seebeck coefficient, ΔV is the difference in the heat potential and ΔT is the temperature difference. Similarly, the magnitude of the Peltier effect can be represented as :

$$\Pi = \frac{Q}{I} \tag{1.2}$$

where Q is the amount of heat that is absorbed or emitted when the current (I) is applied. The relation between S and Π can be expressed as:

$$\Pi = TS \tag{1.3}$$

Finally, the most important parameter is the thermoelectric figure of merit (ZT) :

$$ZT = \frac{S^2\sigma}{k}T \tag{1.4}$$

where S is the Seebeck coefficient, T is the temperature, σ is the electrical conductivity and k is the thermal conductivity. Note that the numerator $S^2\sigma$ is also known as power factor (pf). The equation 1.4 suggests that in order to increase ZT, the material should either have a higher electrical conductivity or a lower thermal conductivity[142]. The thermal conductivity can be further expressed as[143]:

$$k = k_{electron} + k_{phonon} \tag{1.5}$$

where $k_{electron}$ is the contribution from electrons and $k_{phonon}$is the contribution from phonons.

If we now consider equation 1.4 taking equation 1.5 as a reference, neither conductors nor insulators are better for thermoelectric applications. This can be further simplified:

- Case 1: Increase S : but this will reduce electrical conductivity (insulators)
- Case 2: Increase σ: since electrons are also the heat carriers, the thermal conductivity will also increase (metals)
- Case 3: Increase electrical conductivity (σ) without increasing the thermal conductivity (k) (semiconductors)

As a consequence, nanoscale semiconductors are the most promising materials for increasing ZT by decreasing k_{phonon} without affecting $k_{electron}$. Indeed, in the case of nanowires, it is possible to decrease the phonon diffusion along the wire by decreasing its diameter without affecting the electrical conduction and thus, to overcome the bulk limitations. In addition, engineering hetero-interfaces along the wire by implementing Quantum Dots (QDs) or Quantum Wells (QWs) can improve the Seebeck coefficient by increasing phonon-surface scattering. The general idea is to create interfaces that electrons will not notice, and where phonons will scatter[144].

From the material point of view, Si nanowires[145, 146] were intensively studied, and even a CMOS compatible nanoscale generator was reported[141]. The $Si_{1-x}Ge_x$ alloy[147] is also advantageous since it allows to engineer the bandgap, and create axial heterojunctions. However, materials that are historically known for having a high ZT are Bi based chalcogenides such as BiSb[148, 149], BiTe[150], BiSbTe[151], Sb_2Se_3[152] etc. The ZT at nanoscale remains a bottleneck since the highest individual ZT reported for p-type $Bi_{0.5}Sb_{1.5}Te_3$[151] nanowires is 1.14 at 330K and is 1.59 for β-Zn_4Sb_3[153] nanowires at 675K. Considering bulk materials, the highest reported ZT value is 2.4 by Venkatasubramanian et al.[154] in a Bi_2Te_3/Sb_2Te_3 superlattice thin film device.

1.10 Sensors

A sensor is a device that produces a measurable signal in response to the external stimulus. The key parameters of a sensor are: accuracy, resolution, signal-to-noise ratio (SNR), drift, sensitivity, selectivity, stability, recovery over time and range. In this context, using semiconducting nanowires can be advantageous since: (i) the large surface area of nanowire based detectors improves some key parameters like sensitivity and response time, (ii) size, weight and power consumption are improved with nanowire sensors, (iii) the SNR is improved since a lot of wires can be used in parallel[155] and (iv) multiplexing is possible with the help of nanowire arrays[156, 157].

Figure 1.13 presents a schematic of a nanowire based sensor. The sensor uses a large number ZnO nanowires to detect H_2 : when the sensor feels the ambient atmosphere, O_2 molecules are adsorbed at the surface, which yields to the creation of O_2^- and O^- species. This causes a surface depletion of the n-type nanowires, and thus their resistance increases. If the sensor is exposed to a reducing environment such as H_2 , electrons are released from surfaces and transferred to the conduction band. This increases the nanowire conductivity. Similarly, if the environment is composed of oxidizing species such as NO_2, the resistance further increases.

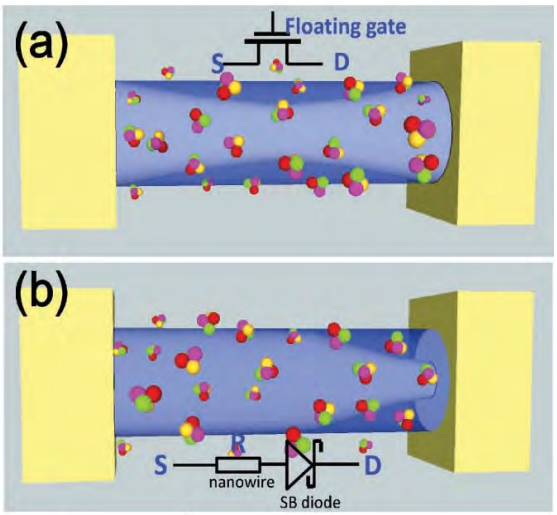


Figure 1.13 – *3D schematic of a nanowire based chemical sensor. (a) conventional FET configuration and (b) the schottky gated configuration . (Hu et al.[158])*

The conductivity of the sensor can be expressed as[155] :

$$G = \frac{\Pi r^2}{l} n_e e \mu_e \tag{1.6}$$

Where G is the conductivity of the nanowire under ambient condition, r and l are the radius and the length of the nanowire respectively, (μ_e) is the electron mobility and (n_e) is the electron density and can be expressed as:

$$n_e = n_0 - \frac{2\alpha N_s}{r} \tag{1.7}$$

where n_0 is the electron density prior to the exposure, N_s represents chemisorbed species, and α is the charge transfer coefficient. The sensitivity is the the ratio of the new conductivity with respect to the original one and can be expressed as:

$$\frac{\Delta G}{G} = \frac{1}{r}\frac{2\alpha N_s}{n_0} \tag{1.8}$$

A direct consequence of this equation 1.8 is that sensitivity is improved when nanowires are thinner.

In order to develop chemical sensors, oxide based nanowires, that are the most stable such as ZnO[159–164], In_2O_3[165,166], SnO_2[167–169], V_2O_5[170], TiO_2[171], and TeO_2[172], have been widely used to detect chemical species including ethanol, NO_2, CO, O_2, NH_3, H_2, etc. Apart from these oxide based nanowires, Pd[173], GaN[174] and Si[175] nanowires have also been used for fabricating sensors. It is also possible to improve the sensor properties such as the response time by using Pd clusters[176] for SnO_2 nanowires, or to develop In[177], Sb[164], Au[178] and Ag[178] doping for SnO_2nanowires. In addition, the sensor robustness can be improved by developing nanowire-based FET structures[160], and optimizing the signal processing[179,180].

On the other hand, silicon is the most used material for building biosensors[181–185] due to its biocompatibility. It is possible to achieve ultra-sensitive probes[186], and to improve the robustness by functionnalizing surfaces or using 3D nanostructures such as nanotrees[187,188].

Chapter 2

Tools and Methodologies

In this chapter, fabrication and characterization tools, that have been used during the thesis, are introduced. The bottom-up integration of III-V nanowires on silicon is carried out by MBE. The morphological characterizations are probed by Scanning Electron Microscopy (SEM). Transmission Electron Microscopy (TEM) is used for crystallography and composition measurements. X-ray Diffraction (XRD) measurements give the macroscopic composition. Finally, the image processing and data treatment methodology are presented and discussed in details.

2.1 The Molecular Beam Epitaxy

Molecular Beam Epitaxy (MBE) is a growth method that can be characterized by the following sentences: "Atomic layer by layer deposition, ultra-high vacuum environment, atomic abruptness, high purity and fewer defects". It is a tool for crystal growth in which atom or molecule beams travel from their source to the substrate in an ultra-high vacuum (UHV) environment. This UHV environment (~ 10^{-11} Torr) ensures that elements travel in collision-free conditions until they reach the substrate, leading to the growth of high quality crystal layers. Furthermore, since the growth rate can be as low as 0.01 monolayer/sec (ML/s), the material can be switched from one to another instantly, leading to ultra-thin interfaces.

In the late 1960s, following the technological breakthroughs in electronics and radiofrequency (RF) devices, the demand for high quality III-V compound semiconductors took a peak. In this context, J. R. Arthur and Alfred Y. Cho from the Bell Telephone Laboratories[189] invented the MBE: a crystal growth technique involving mass transport processes. Within only a few years, MBE got established as a familiar tool not only for high quality crystal growth but also for in-situ characterizations. Some of the MBE achievements include the growth of GaAs / $Al_xGa_{1-x}As$ cascade lasers[190] , the synthesis of high quality GaAs and AlGaAs superlattices[191] and the quantized electron transport[192] in these superlattice interfaces. This opened an experimental door toward nanoscale bandgap engineering and study of quantum mechanisms in condensed matter. In addition, advanced in-situ characterization tools such as the reflection high-energy electron diffraction (RHEED), or the mass spectroscopy measurements can be implemented in the MBE chamber. Moreover, it is possible

to perform surface treatments in the preparation chamber, making thus MBE an ideal platform for studying growth mechanisms.

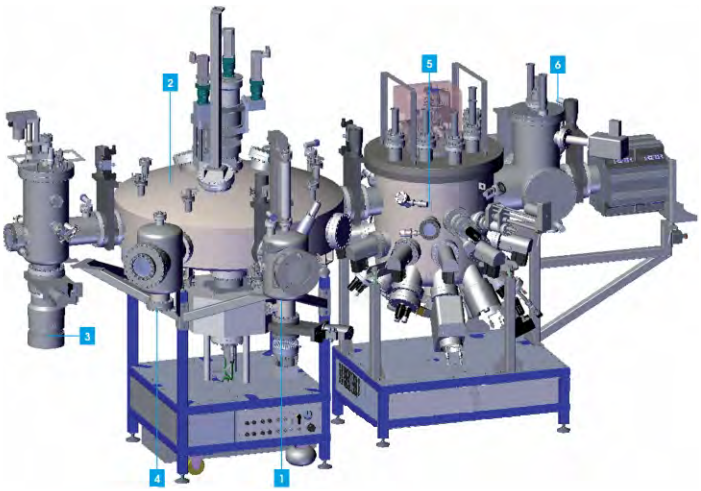


Figure 2.1 – *Riber MBE-412. (1) The loading/unloading chamber, (2) the cluster, (3) the preparation chamber, (4) the parking, (5) the growth chamber and (6) the vacuum system. (http://www.riber.com/assets/files/documentation/mbe412-imp2.pdf)*

The system I used during the thesis for nanowire growth is a MBE-412 from Riber (figure 2.1). It is a multi-chamber system composed of four sections: the loading, the cluster, the preparation and the growth one. The loading, preparation and growth chambers are all connected to the cluster. They are hermetically separated by three electro-valves that grant independent UHV and avoid cross contaminations. This system can be operated in a fully automatic mode thanks to Crystal XE: a software developed and distributed by the manufacturer RIBER. Thanks to "batch recipes", one can program and operate different operations at the same time. This system supports the loading of wafers up to 4 inches. The main features for each chamber is presented in the following sections.

2.1.1 The cluster

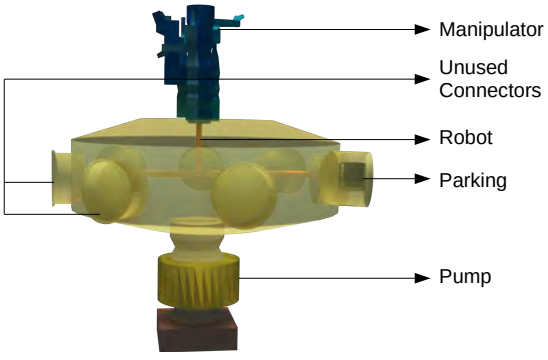


Figure 2.2 – *3D schematic of the cluster. [See real picture in Appendix B figure B.1(b)]*

The cluster is the central part of the system since it allows to transfer wafers between the different chambers thanks to an automated central manipulator (figure 2.2) . For this reason, the vacuum level of this chamber is extremely important and is always below 10^{-9} Torr. In addition, the MBE-412 cluster is equipped with a parking zone, allowing the storage of 5 molyblocks at the same time under UHV conditions. When adding the 10 wafers from the loading, the system can run up to 15 different samples at the same time.

2.1.2 The loading chamber

After ex-situ chemical preparation (if necessary), samples are loaded inside the MBE system via the loading chamber. The figure 2.3 shows a sketch of this chamber. Up to 10 wafers can be loaded at the same time in the system. An elevator equipped with a laser barrier allows the automatic detection of each moly-block loaded in the system. The UHV environment is achieved thanks to a turbo molecular pump (Varian Turbo-V 551 Navigator), combined with a membrane one. Once wafers are loaded, a pressure of $5x10^{-7}$Torr can be reached within 15 minutes.

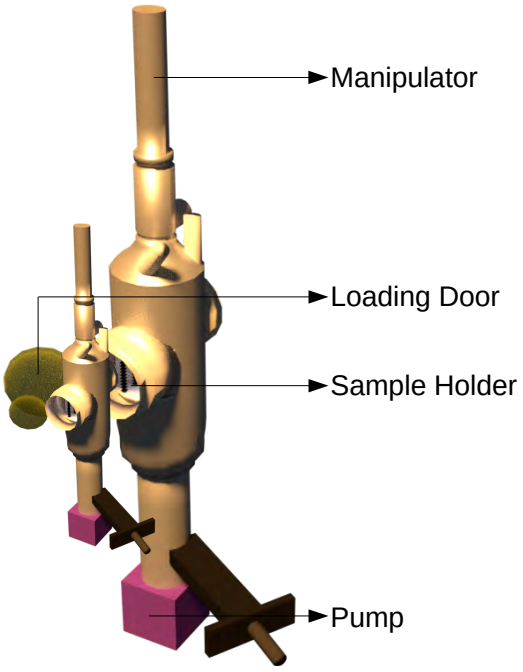


Figure 2.3 – *3D schematic of the loading chamber. [See real picture in Appendix B figure B.1(a)]*

2.1.3 The preparation chamber

Figure 2.4 presents a 3D sketch of the preparation chamber. The purpose of this chamber is to degas the loaded wafers at an elevated temperature, so that the surface contamination is highly minimized before introduction into the growth chamber. The heating is provided by a series of coil resistances behind the substrate, and a temperature of 750°C can be reached. The UHV environment is obtained independently in this chamber using the equivalent pumping configuration than described for the loading.

In addition to this standard configuration, an in-situ H_2 gas / plasma radio-frequency (RF) source is integrated in this chamber (see figure 2.4) for surface preparation. In our setup, the high quality hydrogen is supplied thanks to a H_2 bottle having a pressure of 40 bar. The pressure is then regulated thanks to both: a pressure regulator and a Mass Air Flow (MAF) controller. The RF cavity, positioned between the MAF controller and and the preparation chamber allows separation of H_2 into atomic atoms. This plasma cell is turned off if the desired treatment is H_2 gas; whereas the cell is ignited with proper RF power for H_2 plasma treatment. A manual valve separates the plasma cell and the preparation chamber, and is only opened during surface treatment . More details on H_2 treatments can be found in Appendix A.

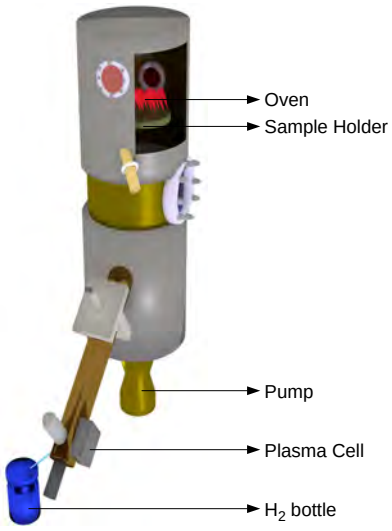


Figure 2.4 – *3D schematic of the preparation chamber. [See real picture in Appendix B figure B.1(c)]*

2.1.4 The growth chamber

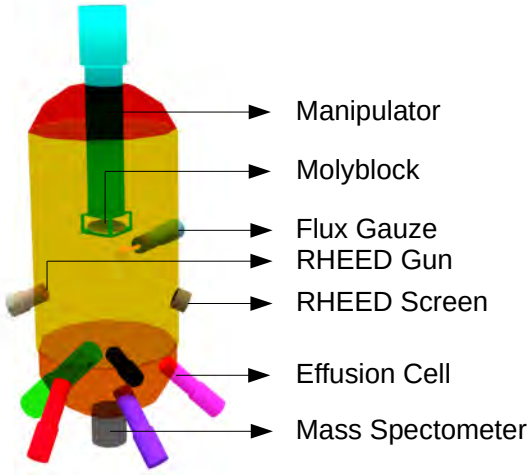


Figure 2.5 – *3D schematic of the growth chamber. See real picture in Appendix B figure B.1(d)]*

The growth chamber is where the material deposition takes place (figure 2.5). The UHV environment is achieved thanks to a Cryo-Torr 8 Cryopump and an ion pump. A cryopanel placed inside the reactor, and filled with liquid N_2, allows to improve further the vacuum level and thus reduces the contamination level of deposited materials. A sample holder controlled by an automated manipulator is located at the center of the chamber. This manipulator rotates at a controlled speed (typically 13 rotations per minute) so that inhomogeneities in the deposition process are avoided. Three spectroscopy tools are present: a flux gauze (above sample holder), a mass spectrometer (at the bottom of the reactor) and RHEED system (gun and display panel are facing each other). The flux gauze is used before each growth in order to calibrate fluxes. The RHEED system allows to measure the growth rate and probe the crystalline structure of the nanowires. The degassed wafers are facing the cells downwards during growth. The temperature is monitored by a thermocouple positioned at the center of the circular heating coils and about 1 cm far from the wafer surface.

The element III sources are standard Knudsen cells (k-cells) and are placed at the bottom hemisphere of the reactor facing upwards. The angle between each source and the sample holder is 45°. Note that a k-cell (figure 2.6) consists in an effusion evaporator source, whose flux is controlled by temperature. The III elements are loaded inside a crucible and two thermocouples measure the base and tip temperatures for each cell (figure 2.6). In both cases, a Proportional–Integral–Derivative (PID) controller allows to perfectly stabilize and control the temperature in each zone.

Figure 2.6 – *Image of standard Knudsen cells. (www.riber.fr)*

On the other hand, cracker cells are mostly used for evaporating group V elements (i.e.: As and Sb). The reason is because group V elements are generally evaporated in tetramer forms, whereas dimers are preferred for crystal growth. Indeed, lower defect levels and better material quality are achieved using dimer sources[189], which explains the necessity of the cracker zone to transform tertramers into two dimers. Moreover, the cracker cells are equipped with a digital electro-valve allowing full control of the valve opening, and thus a full control of the group V flux (up to 0.01%). Finally, fast changes of the element V flux are possible compared to standard effusion cells limited by the thermal inertia of the source.

The growth chamber is also equipped with a RHEED system (kSA 400), which allows in-situ flux calibrations and structural characterizations. In a RHEED, a collimated mono-energetic electron beam from the RHEED source is directed towards the substrate surface at a grazing angle of about 1° with an energy that lies between 5 – 40 keV. As a consequence, the penetration depth of this beam is limited to the first few atomic layers and, since the energy component perpendicular to the substrate is in the order of 100 eV, creation of defaults is avoided. A CCD camera collects the reflected beam at the opposite side of the electron gun and record the diffraction pattern. The intensity of this pattern oscillates as a function of the surface roughness (figure 2.7). A fully flat surface shows an intensity maximum, while the minimum is observed when half of the next monolayer is grown (see figure 1.6). From the oscillation frequency, it is thus possible to determine the growth rate, which gives an absolute reference for flux calibrations of each III and V element. Using the flux gauge of the system, it is then possible to calibrate fluxes before starting any growth session using Beam Equivalent Pressures .

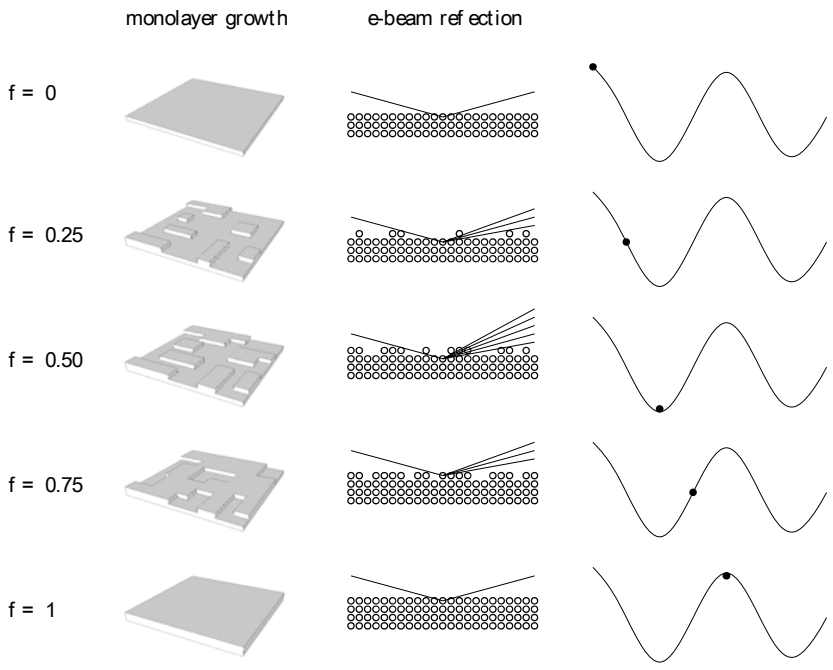


Figure 2.7 – *RHEED Calibrations. (Arthur[189])*

2.2 The electron microscopy

"An electron microscope is a microscope that uses a beam of accelerated electrons as a source of illumination. As the wavelength of an electron can be up to 100,000 times shorter than that of visible light photons, electron microscopes have a higher resolving power than light microscopes and can reveal the structure of smaller objects."[193] Indeed, the wavelength of visible light is in the range 400−700 nm, which limits possible observations of nanostructures (smaller visible structures ~300 nm).

From a theoretical point of view, the wavelength of a particle (electron in this case) with a mass (m) and an energy (E) can be expressed as :

$$\lambda = \frac{h}{\sqrt{2mE}} \tag{2.1}$$

where h is the Plank's constant.

In the case of electrons, the considered wavelength can be controlled thanks to the acceleration energy, making them ideal source for nanoscale microscopy. In an electron microscope, the magnification power can be 100,000 times higher than in an optical one. Furthermore, since electrons have mass and charge, they can interact with the studied material and give additionnal informations. Indeed, when interacting with the underlying surface, several components can emerge as presented in figure 2.8. Each of these signals carries different information about the sample and, with adapted tools and filtering techniques, it is possible to measure the crystalline structure, the topography, the strain mapping or the composition of the nanoscale materials.

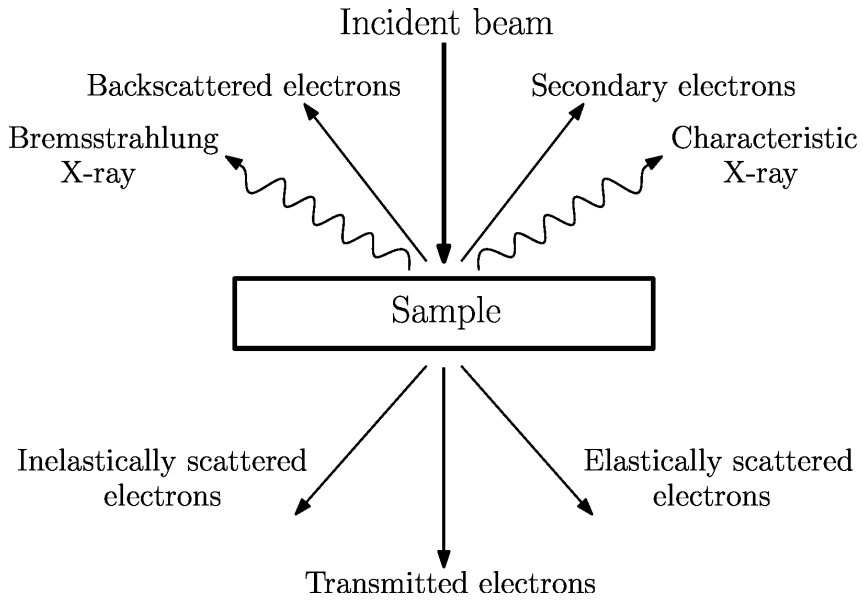


Figure 2.8 – *Electron Matter Interactions*

In the particular case of a scanning electron microscope (SEM), images are generated from electrons scattered around the surface: backscattered and secondary electrons. SEM provides thus informations related to the surface of the studied material such as the morphology or the composition. In contrast, a transmission electron microscope (TEM) generates images using electrons crossing the sample, and that could have undergone elastic or inelastic scattering. In that case, informations such as cystal phase, composition, growth direction, interface abruptness and crystal quality can be obtained. SEM and TEM are thus two complementary tools allowing full nanoscale characterization of our samples.

2.2.1 The scanning electron microscope

As mentioned previously, a SEM is a tool typically used to inspect the topography of samples at nanoscale. The SEM working principle is that a focused beam of electrons scan the sample surface; the electrons interact with atoms close the surface and the re-emitted signal (secondary electrons) is collected with a positively biased detector. The SEM image is produced by sweeping the sample area with the electron beam. When changing the acceleration voltage of electrons (typically between 1kV to 40kV), it is possible to focus observations on either morphology (low acceleration voltages) or chemistry (high acceleration voltages). Indeed, the electron penetration depth in the sample depends directly of their energy. The quantity of secondary electrons collected increases with the acceleration voltage up to the point where they recombine before they can reach the surface. Furthermore, it also is possible to collect backscattered electrons (BSE). BSE are high-energy electrons that are reflected or backscattered by elastic scattering interactions with the sample atoms. The emitted quantity of BSE depends directly of the atomic number of the scanned elements: heavy elements (high atomic number) backscatter electrons more strongly than light elements (low atomic number), and thus appear brighter in the image.

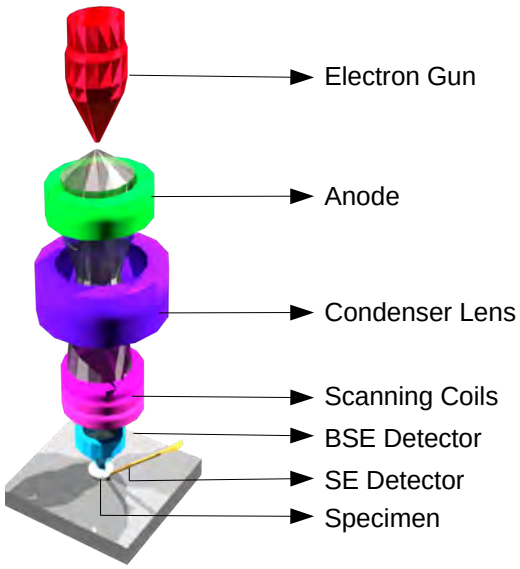


Figure 2.9 – *3D schematic of the Scanning Electron Microscope*

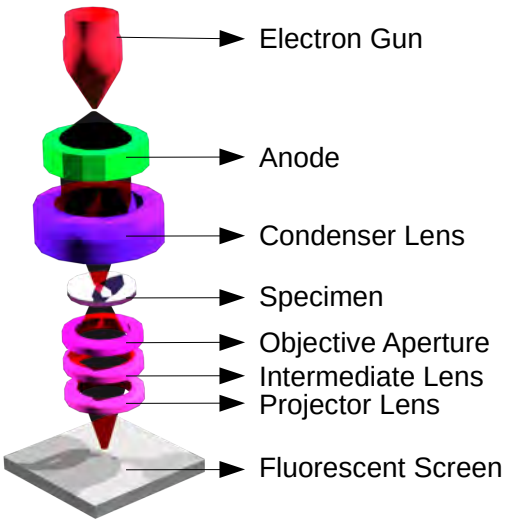
In a typical SEM, which schematic can be seen in figure 2.9, an electron beam is generated by field emission effect from a cathode (shaped as a small tip) and is accelerated towards an annular anode by a negative potential of 1-40 kV. The beam is then aligned thanks to electro-magnetic lenses placed at the center of the column: a first system of lenses focus the beam into a narrow diameter of a few nanometers; and then a second system of lenses, called objective lenses, takes care of the magnification, focus and aberration corrections. In between, a couple of coils are designed to

move quickly the beam across the specimen in order to scan it pixel by pixel. Different types of detectors collect respectively secondary and backscattered electrons produced by the beam-sample interactions. An analysis system, triggered with the scan speed, rebuild an image using amplitudes of the collected signals. The full system is kept under an high vacuum environment thanks to a turbo-molecular pump in order to protect electrons from interactions before reaching the sample.

Due to its working principle, the SEM resolution (1-20 nm) is not limited by the wavelength of the incident electrons, but rather by the incident beam properties and the electron-matter interactions. Considering the incident beam properties, the resolution limiting factor is the beam diameter, which depends mostly on spherical, chromatic and astigmatism aberrations. A spherical aberration is an "on-axis" aberration which arises when the lens focus depend of the lateral position. A chromatic aberration occurs if the electrons in the beam are not perfectly mono-energetics. Astigmatism occurs when the magnetic field of the lens is not homogeneous in plane. While chromatic aberration can be minimized using modern electron sources such as cold field emission guns and astigmatism can be corrected using stigmators, the spherical aberration is intrinsic to the lens.

In this thesis, we used for characterizations a FEI Helios Double Beam 600i equipped with a Schottky FEG (declared resolution of 0.9 nm at 15 k) and with a LMIS Gallium source to perform Focused Ion Beam (FIB) processes.

2.2.2 The transmission electron microscope



(a) *Transmission Electron Microscopy*

Figure 2.10 – *3D schematic of the Transmission Electron Microscope*

TEM is an important invention for material characterizations and was awarded with noble prize in 1986. Its resolution is about 1 Å. In a TEM, the electron beam with a very high energy (typically in the range of 100 kV) is crossing the sample, which is 100nm thick at maximum. Therefore, electrons can either pass through the sample without having any interaction or undergo elastic interactions with sample atoms. These interactions are used to get the morphological, crystallographic and compositional information about the sample. The schematic in figure 2.10a reports the typical TEM architecture. A high energy electron beam is generated from the electron gun. This beam is aligned thanks to condenser lenses, afterward crosses the sample and the objective aperture, is collected by the intermediate lenses and is imaged on a fluorescent screen for analysis thanks to the projector lenses.

From the fundamental point of view, if we consider electrons as waves and not particles, it is possible to use the Bragg's law (figure 2.11) to describe the interactions between the incident beam and a crystalline sample. In that particular case, the diffraction of electrons only occurs in precise directions, which are characteristic of the sample crystalline structure. It is thus possible, collecting this diffracted pattern, to characterize the structure of the studied sample.

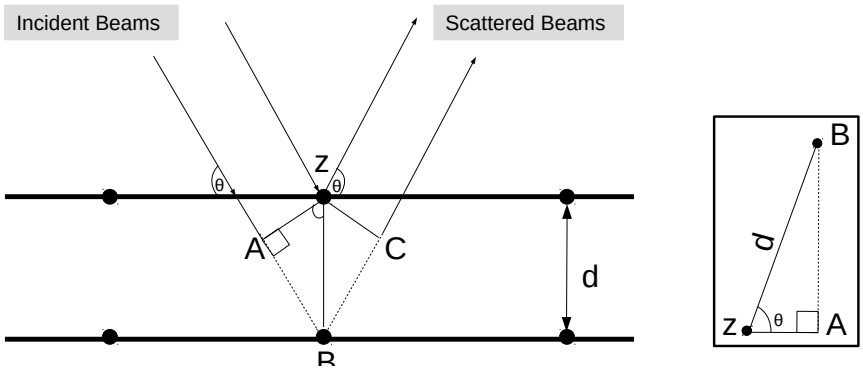


Figure 2.11 – *Illustration of Braggs law. Image Source (http://skuld.bmsc.washington.edu/~merritt/bc530/bragg/)*

The Bragg's law can be written as follow:

$$2dsin(\theta) = n\lambda \tag{2.2}$$

where λ is the wavelength of electrons, d is the distance between atomic layers in the crystal and θ is the diffraction angle.

When d is small the equation 2.2 can be written as:

$$\theta = \frac{\lambda}{2d} \tag{2.3}$$

In this thesis two TEM have been used: a JEOL JEM-2100F with a declared resolution of 2.3 Å at 200 kV and a JEOL JEM-ARM200F with a declared resolution of less than 1.9 Å at 200 kV .

2.3 The X-Ray diffraction

The XRD, also known as X-Ray diffraction, is a powerful tool for crystal characterizations and is commonly used for identifying crystal structures, compositions and lattice parameters. The fundamental working principle is the same than for TEM: it is based on the Bragg's law and the diffraction of X-Rays by the crystal (see equation 2.2 and 2.3). The X-rays wavelength is in the order the Angstrom (10^{-10}m), which is the typical distance between atomic planes in a crystal. When X-Rays interact with a crystalline lattice, a diffraction pattern is formed which reveals the spacing between atomic planes and thus allows structural and compositional determination.

The figure 2.12 presents the 3D schematic of the X-ray diffractometer that was used during this thesis. The main components of a diffractometer are:

1. **The source:** The X-Rays are generated in a cathode ray tube by heating a filament to produce electrons. These electrons are then accelerated toward a target material. If their energy is high enough, they can dislodge inner shell electrons from the target material (Cu, Fe, Mo, Cr), and thus produce a characteristic X-Ray spectra. Depending of the element, the emitted radiation is categorized as a $K_{\alpha 1}$, $K_{\alpha 2}$ or $K_{\beta 1}$line.

2. **The primary optics:** The role of the primary optics is to prepare X-Rays before reaching the sample. It is composed of three elements: the soller slits to keep the beam in plane, narrow and symmetric, the divergence slits to control the width and avoid divergences and the monochromator to select only a wavelength ($K_{\alpha 1}$, $K_{\alpha 2}$ or $K_{\beta 1}$).

3. **The stage :** The stage is where samples are placed. It can rotate in 3 directions.

4. **The secondary optics:** The secondary optics has four main components namely: the anti-scatter slit which reduces the divergence height and the diffusely scattered rays, the soller slit which reduces axial divergence and limits beam height, the receiving slit which removes the diffracted and scattered x-rays, and monochromator whose role is to select one wavelength.

5. **The detector:** The detector allows detection of diffraction patterns.

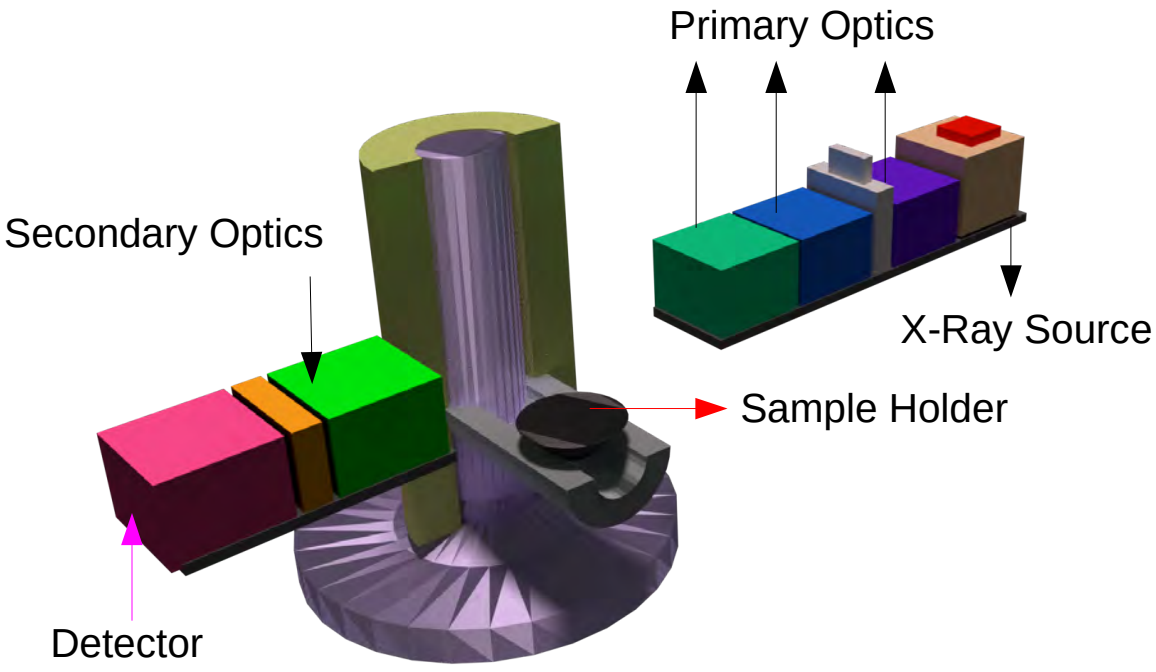


Figure 2.12 – *3D schematic of the XRD diffractometer*

2.4 The statistical analysis of nanowires

One of the critical task during the sample analysis is to get a proper statistical description of the wafers. This task becomes tedious once the number of sample increases, and manual measurements are a possible source of errors. For this reason, we developed a semi-automatic image processing and a fully automatic data analysis methodology, using well known open source software. This section provides an overview of the image and data treatment processes.

2.4.1 The image processing

Figure 2.13 summarizes the different image processing steps that were carried out using Fiji,[194] an open source software. The figure 2.13 (a) presents a typical SEM image of an as-grown sample. Next is the image segmentation to avoid overlap of nanowires with each other. If there is overlapping, nanowires should be separated from each other manually, ensuring that length and diameter are not lost [see figure 2.13 (b)]. The next step of the segmentation [figure 2.13 (c)] which involves image inversion followed by thresholding. Image inversion ensures nanowire (in black after inversion) and background (white after inversion) separation during thresholding. The particle detection follows next [figure 2.13(d)], and allows the detection of each nanowire present on the wafer. The nanowire ellipse fitting during particle detection provides a measurement of the major axis (length), the minor axis (diameter) and the angle between both axes (verticality). This angle measurement ensures that only vertical nanowires are present in the data file for further analysis.

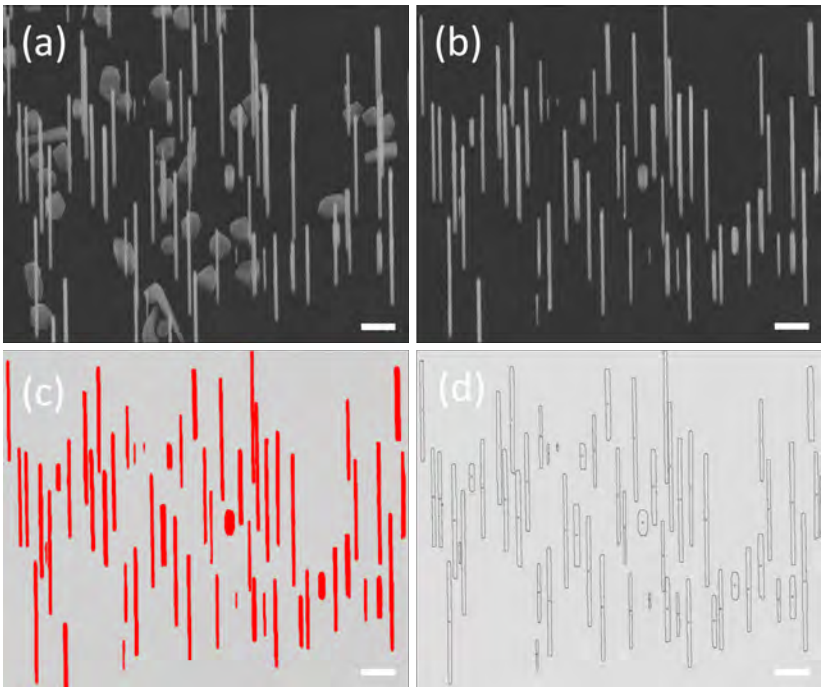


Figure 2.13 – *Image Processing Steps. (a) Orignal SEM image, (b) image segmentation: separating overlapping nanwires, (c) image inversion and thresholding and (d) particle detection. Scale bars are 500nm.*

2.4.2 Data Analysis

The process flow chart (figure 2.14) represents the data treatment and analysis that follows the image processing part . It was carried out with Rplatform[195] using Rstudio[196] as an Integrated Development Environment (IDE). Additionally, two packages dplyr[197] and ggplot2[198] were further implemented during the process to facilitate respectively the data analysis and the plotting.

First, diameter and length were calculated for at least 150 nanowires present in the data file using the major axis, minor axis and the angle values, and the following equations:

$$Diameter = MinorAxis \tag{2.4}$$

$$Length = 2 \times (MajorAxis - MinorAxis) \tag{2.5}$$

The factor 2 in the equation 7 comes from the 30° tilt angle used during SEM measurements.

Finally, measured angles between 85° and 95° were the only considered ones to ensure that only fully vertical nanowires are integrated in the statistic file. Nanowires are then categorized in 6 different families based on their diameter (0-60, 61-120, 121-180, 181-240, 241-300 and 301-360 nm). For each group, average length, diameter, and probability of occurrence are calculated based on the total number of nanowires present on the sample. Furthermore, an average length and diameter is measured for each sample based on weighted average probabilities. From this, probability and line plots are build for each family, while the scatter plot is based on every vertical nanowires present on the wafer (see statistics in chapter 4).

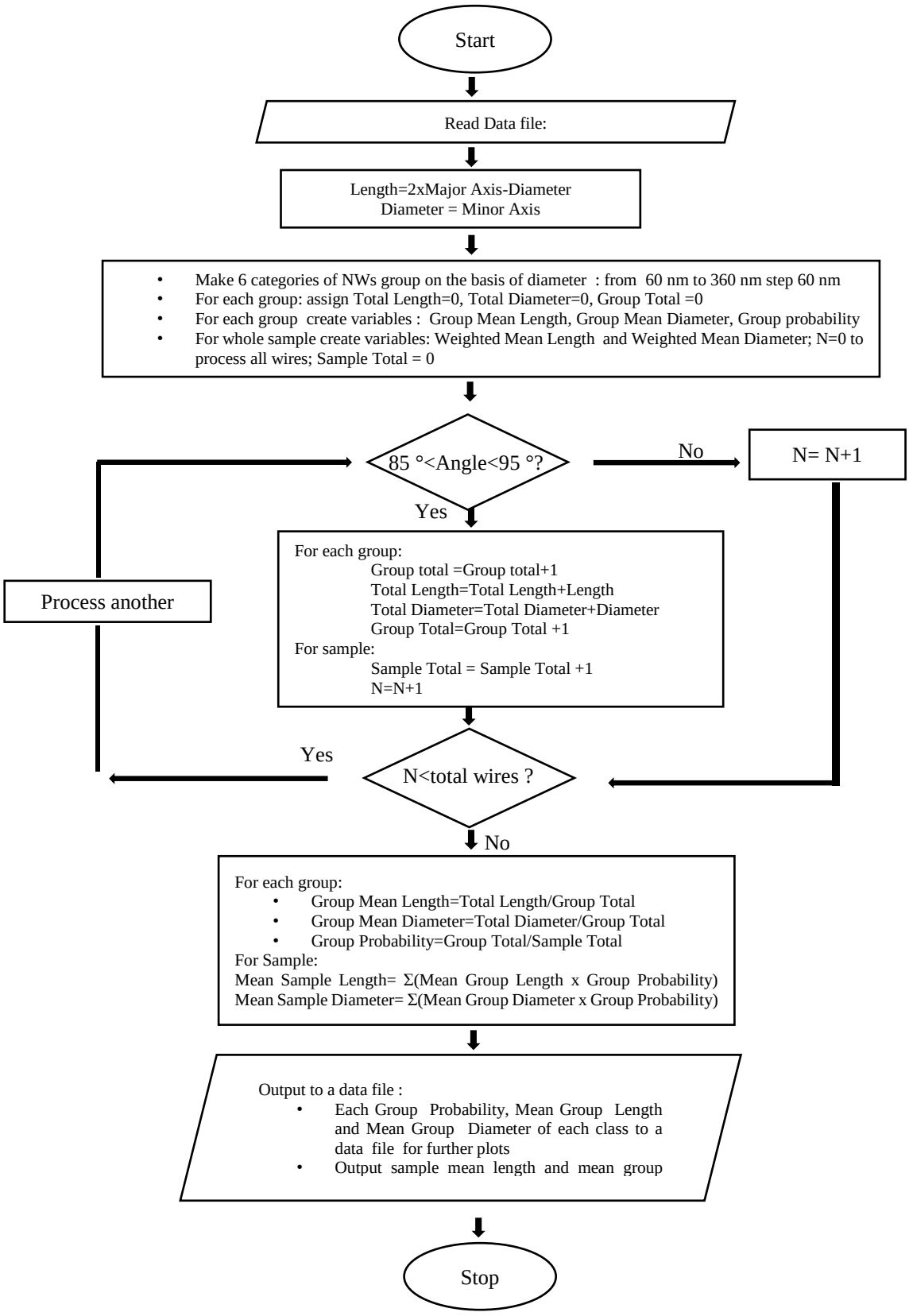


Figure 2.14 – *Data Treatment Flowchart*

Chapter 3

The Nanowires Growth Mechanisms

"Epitaxy" originates from two Greek words: "epi" meaning above and "taxi" meaning "in an ordered manner". In material science, "Epitaxy" means thus the growth in an order manner of a crystal on top of another one. The three key ingredients controlling the process are the substrate over which the deposition takes place, the materials that will be grown and the environment during epitaxy. It can either be called homoepitaxy when the grown material and the substrate are the same, or heteroepitaxy when both materials are different. While the process is simple for the former, the stress induced by the lattice mismatches in the latter becomes crucial and needs to be accommodated.

In the particular case of nanowire growth, the epitaxial process is controlled by the growth temperature, the flux of each evaporated material, the ratio of material with respect to each other, the growth time, the surface preparation and the catalyst nature. The classical procedure for controlling the epitaxial process is to first prepare the substrate surface (remove oxide, create patterns) and deposite the metal catalysts (control the density and diameter). The growth temperature is then fixed and finally the flux of each material is optimized. The reason for fixing the growth temperature first is that this parameter has the biggest influence on crystal growth, and is also influencing the other ones. The other parameters listed before are then optimized in order to control the nanowire morphology (length and diameter), the growth direction and the density.

The nanowires growth process can be divided in three steps: first the nucleation followed by a transition regime before reaching the steady states. The nucleation deals with early stages of nanowire growth and the uprising of the droplet above the substrate. The transition regime deals with the change of the material collection area on the substrate surface. The steady state regime deals with the equilibrium that is reached when growth does not depend of the substrate surface anymore. Hence, it is necessary to engineer this growth process, which is thermodynamically and kinetically driven, in order to have full control over morphology, density, crystalline structure and composition of nanowires.

The objective of this chapter is to present the global theory behind III-V nanowire growth and to unveal its fundamental physics. The first section focuses on two standard growth mechanisms for III-V nanowires: the Vapor-Liquid-Solid (VLS) and Vapor-Solid (VS) one. Next, the possible III-V nanowire crystalline structures are discussed: Zinc Blend (ZB) and Wurtzite (WZ). Finally, insights on Density Functional Theory (DFT) simulations are given for understanding surface preparations.

3.1 The VLS growth mode

The VLS growth mechanims is the standard one for III-V nanowire growth. It was first reported by Wagner and Ellis[1] in 1964 to synthesize silicon whiskers. The process involves the formation of a metallic droplet before growth that serves as a physical or a chemical catalyst. These nanoparticles are modifying the surface chemical potential and thus allow the collection of materials. They are a key ingredient for promoting nanowire nucleation and then the vertical growth. The most widely used metal to act as a catalyst is gold since it does not oxidize in air, and it forms eutectic alloys with a lot of materials: Ge, Si, In, Ga, Al, Zn ... etc. In addition, it is possible to control the size and the density of nanoparticles by either using gold colloids or dewetting of a thin gold layer. Despite the high degree of control over nanowire morphology and density that Au mediated growth offers, it is prohibited for some applications such as Nanoelectronics. Indeed, gold is a deep level impurity in silicon, creating mid-gap defects in the band structure, and thus degrading the electrical and optical device properties. Therefore, two options are possible for growing CMOS compatible III-V nanostructures on silicon: either using a self-catalyzed growth mechanism or using a third party metal catalyst compatible with CMOS such as Ag, Pt, or Pd . Furthermore, the self-catalyzed growth can either be assisted by a droplet, where an element III (Ga or In) takes the role of gold, or can occur thanks to a VS or a Selective-Area growth process. In the former case, metallic droplets are deposited in-situ prior to nanowire growth, whereas in the later case substrates can be pattern beforehand.

Since the goal of using a catalyst is to change the chemical potential on the substrate surface and to promote nanowire growth by collecting materials, the condition for VLS growth to occur is that the Vapor-Solid chemical potential is higher than the Vapor-Liquid one. With this condition, it is favorable for materials at the substrate surface to travel to the droplet and be collected[199].

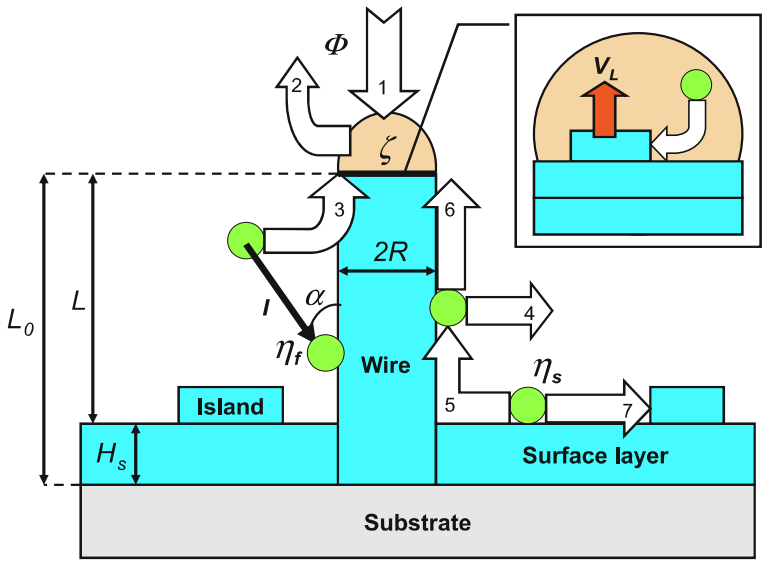


Figure 3.1 – *Kinetics of the VLS mechanism. (Dubrovskii[199])*

Figure 3.1 summarizes the main kinetic processes that are involved during the VLS growth in a MBE system. The growth is driven by the incident fluxes (I) that create the vapor saturation Φ. The process 1 corresponds to the direct impingement of atoms on the droplet surface and the process 2 represents the material desorption at the Vapor-Liquid interface. In addition to these direct processes, atoms can also be collected from the nanowire sidewalls (process 3) and diffuse to the droplet (process 6), or be desorbed laterally (process 4). Finally, it is also possible to collect material from the substrate surface for nanowire growth (process 5) or for bulk/layer growth (process 7). The VLS mechanism occurs when the quantity of material entering the droplet is higher than the quantity of material leaving. It is then possible for the droplet to reach the supersaturation and thus to grow a crystal underneath (at the Liquid-Solid interface). In that case, a nuclei is formed either at the center of the droplet or at the triple phase boundary depending of the nanowire diameter and the growth conditions as shown in figure 3.2 (a)[200] . Finally, a new layer is formed below the droplet, originating from the nuclei, by crystallization of the supersaturated catalyst. This process repeats with the refilling of the droplet, which finally lead to nanowire growth [see figure 3.2 (b,c and d)]. The droplet remains in general visible at the top of the nanowire during the morphological characterizations.

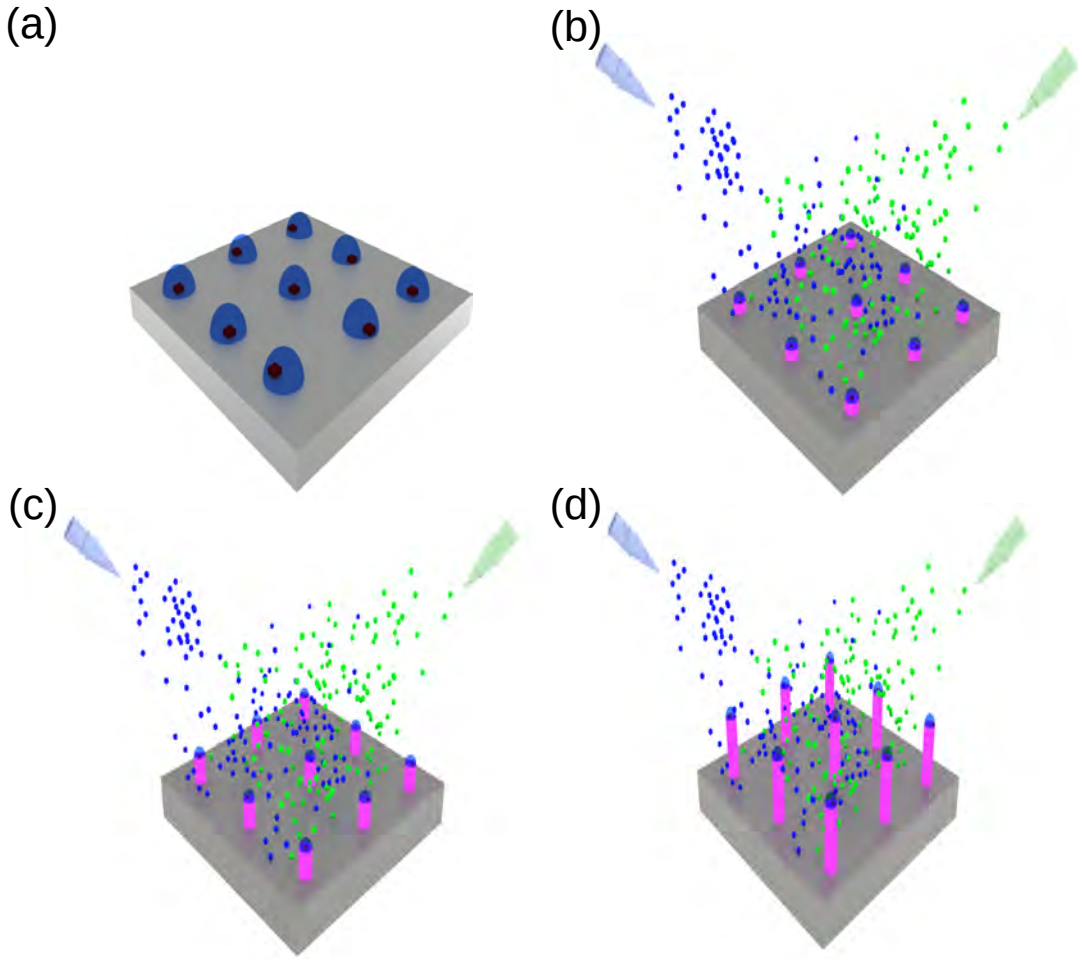


Figure 3.2 – *3D Illustration of the (a) nucleation followed by (b-d) growth of nanowires.*

The VLS process can be understood thanks to the phase diagrams: an example of the Au-Si system is presented in figure 3.3. The Au catalyst forms a liquid Au-Si alloy when the temperature is raised above the eutectic point (~361 °C). This alloy formation is characterized by a solid to liquid phase transition (see region AB in figure 3.3). Once the growth temperature is reached, the supply of Si atoms allows supersaturation of the droplet (C) and finally lead to a new nucleation (region BCD in figure 3.3). After nucleation, the bilayer quickly covers the whole liquid/solid interface, forming a new section of nanowire. By repeating, this process allows nanowire growth.

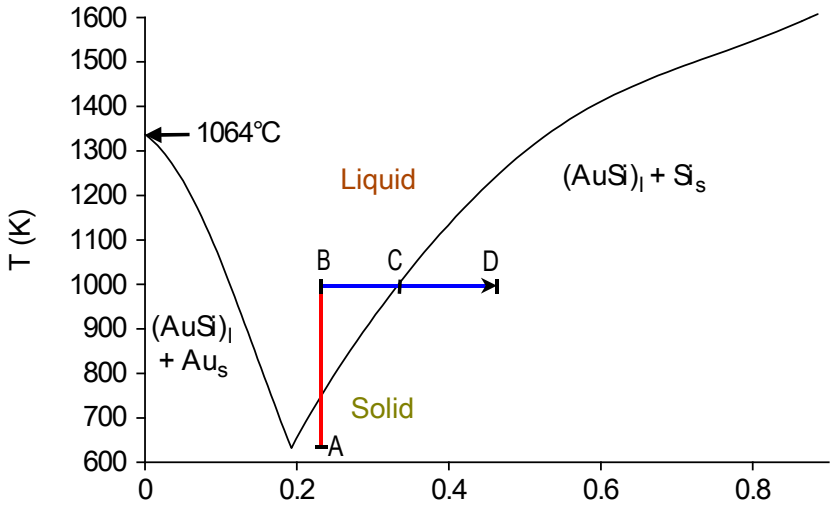


Figure 3.3 – *Au–Si system with ∼18% solubility of Si in Au. (Adapted from Mayyappan[6])*

3.1.1 Thermodynamic Considerations

3.1.1.1 Gibbs-Thomson Effect

The formation of a molten metal droplet can be explained by the minimization of its free energy. The Gibbs-Thomson effect describes the chemical potential increase in a particular phase, due the Laplace pressure, which results from curvature effects. Indeed, if for example a liquid material (blue sphere in figure 3.4) having a surface S, a pressure P_l and a Volume V_l is surrounded by a gaseous material (green in figure 3.4) having a pressure P_g and volume V_g , the pressure difference between these two phases (dF) can be written as[199]:

$$dF = \gamma dS - P_l dV_l - P_g dV_g \tag{3.1}$$

where γ is the surface tension of the liquid/vapor interface.

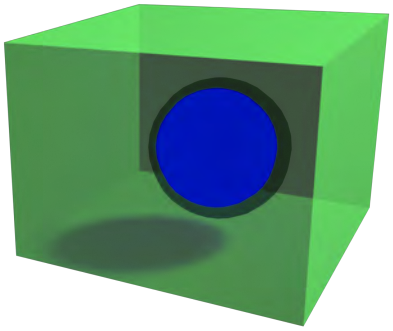


Figure 3.4 – *Laplacian Pressure*

If the considered system is at the equilibrium, volumes are equal but of opposite signs,

$$dV_g = -dV_l \tag{3.2}$$

and the Laplacian pressure is constant, so $dF = 0$ in equation 3.1.
It results that :

$$P_l - P_g = \gamma \frac{dS}{dV_l} \tag{3.3}$$

where γ is the surface energy of the droplet and dS is the surface change.

"In thermodynamics, the Gibbs free energy, also known as free enthalpy is a thermodynamic potential that can be used to calculate the maximum of reversible work that may be performed by a thermodynamic system at a constant temperature and pressure (isothermal, isobaric)".[201] It is expressed as:

$$G = H - TS \tag{3.4}$$

where H is the enthalpy, T is the temperature and S is the entropy. The enthalpy of a thermodynamic system is defined as:

$$H = U + pV \tag{3.5}$$

where U is the internal energy of the system, p is the pressure of the system and V is the volume of the system.

From equation 3.4 and 3.5,

$$G = U + pV - TS \tag{3.6}$$

The derivative of equation 3.6 gives

$$dG = dU + pdV + VdP - TdS - SdT \tag{3.7}$$

For a closed system, $dU = TdS - pdV$. Hence, equation 3.7 becomes

$$dG = VdP - SdT \tag{3.8}$$

In the case of a fixed temperature, the second term of equation 3.8 ($SdT = 0$), and thus

$$dG = VdP \tag{3.9}$$

The integration of equation 3.9 gives,

$$\int_{G_0}^{G_\infty} dG = \int_{P_0}^{P_\infty} Vdp \tag{3.10}$$

or,

$$G(p_\infty) - G(p_0) = \int_{P_0}^{P_\infty} Vdp \tag{3.11}$$

From the ideal gas equation, $pV = Nk_BT$, where p is the pressure, V is the volume , N is the number of gas molecules, k_B is the Boltzmann constant and T is the temperature, equation 3.11 can be simplified as $(N = 1)$:

$$G(p_\infty) - G(p_0) = k_B \int_{P_0}^{P_\infty} Vdp \tag{3.12}$$

$$= k_BTln\left(\frac{P_\infty}{P_0}\right) \tag{3.13}$$

In the particular case of a liquid droplet on a planer surface (see figure 3.5):

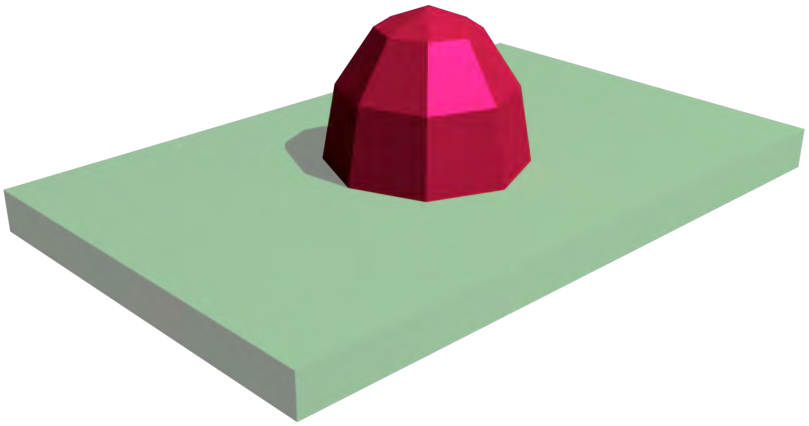


Figure 3.5 – *Curved surface on a planer surface.*

The change of free enthalpy (dG) after transferring one atom from the vapor to the liquid droplet can be written as:

$$dG = \mu_l - \mu_v \tag{3.14}$$

or,

$$dG = \mu_{l\infty} + \gamma dS - \mu_v \tag{3.15}$$

where μ_l and μ_v respectively are liquid and vapor chemical potential. $\mu_{l\infty}$is the chemical potential of a surface of infinite radius, γ is the surface energy of the droplet and dS is the surface change.

In the particular case presented in figure 3.5 (liquid droplet of radius R_{drop} on a surface), it can be written as:

$$dS = \frac{2dV}{R_{drop}} \tag{3.16}$$

where dV is the volume change and R_{drop} is the droplet radius.

From equations 3.14 and 3.15,

$$\mu_l - \mu_v = \mu_{l\infty} + \gamma dS - \mu_v \tag{3.17}$$

or

$$\mu_l - \mu_{l\infty} = \gamma dS \tag{3.18}$$

From equations 3.16 and 3.18,

$$\mu_l - \mu_{l\infty} = \frac{2\gamma dV}{R_{drop}} \tag{3.19}$$

From equation 3.19, the Gibbs-Thomson equation for the difference in chemical potential (μ) between a curved surface (radius, l) and planar surface (radius, l = ∞) as shown in figure 3.5 can be written as:

$$\mu_l - \mu_{l\infty} = \frac{2\gamma\Omega}{l} \tag{3.20}$$

where γ is the surface energy of the droplet and Ω is the molar volume of the species within the nuclei.

The above equation 3.20 can be used to describe the critical diameter of a pure phase nuclei and the vapor–liquid equilibrium differences for spherical droplet and the planar surface represented in figure 3.5. Assuming the same reference state for gas-phase species, one can express chemical potential of gas-phase species in terms of partial pressures.

At equilibrium, the chemical potentials are given by:
For the droplet

$$\mu_l = \mu_g \tag{3.21}$$

and for the planar surface

$$\mu_{l\infty} = \mu_{g\infty} \tag{3.22}$$

Subtracting equation 3.22 from equation 3.21 and considering an ideal gas solution ($\mu_{g\infty}$=0) ,

$$\Delta G = \mu_{l\infty} - \mu_l = \mu_{g\infty} - \mu_g = -\mu_g \tag{3.23}$$

From equations 3.23 and 3.13:

$$-\mu_g = k_B T ln[\frac{p\infty}{p}] \tag{3.24}$$

or,

$$\mu_g = k_B T ln[\frac{p}{p\infty}] \tag{3.25}$$

where $\frac{p}{p\infty}$ represents the vapor-phase supersaturation within the gas phase, k_B is the Boltzmann constant, and T is the temperature. Using equations 3.20 and 3.25, the concentration (partial pressure, p) of the gas phase in equilibrium with a liquid droplet of known size is given as:

$$k_B T ln[\frac{p}{p\infty}] = \frac{2\gamma\Omega}{r} \tag{3.26}$$

It can be observed that the partial pressure of the species has to be in equilibrium. One can write the partial pressure of gas-phase solutes that will be in equilibrium with a droplet of radius, r, P_r as following:

$$P_r = P^\infty e^{\frac{2\gamma\Omega}{rk_B T}} \tag{3.27}$$

where P^∞ is the partial pressure of the gas-phase solutes in equilibrium with a planar surface. One can also interpret the above equation for estimating the critical nucleation for pure phase condensation (say, molten metal droplets from metal vapor).

$$r_c = \frac{2\gamma\Omega}{RT ln[\frac{p}{p\infty}]} \tag{3.28}$$

Here r_c is the critical size of nuclei. Supersaturation, in this case, can be varied by changing the partial pressure, p.

3.1.1.2 Nucleation from Molten Metal Alloy Droplet

Nucleation of a solid-phase growth species out of a spherical metal droplet is shown in figure 3.5. Thermodynamically, Gibbs free energy minimization is the criterion to satisfy. Gibbs free energy change for the formation of the nuclei is expressed as

$$\Delta G_T = \Delta G_v . \frac{4}{3}\pi r^3 + \Delta G_s 4\pi r^2 \tag{3.29}$$

where the first term on the right is the free energy change due to change in volume and the second term is the effect of the curvature on the nucleus determined by the created surface area. The nuclei growth is thermodynamically favourable if and only if $\Delta G_T < 0$.

The critical nuclei size can be estimated from the condition:

$$\frac{\partial \Delta G_T}{\partial r} = 0 \tag{3.30}$$

This leads to the expression for critical radius r * as

$$r* = \frac{-2\sigma}{\Delta G_V} \tag{3.31}$$

where r * is the critical nuclei radius σ is the interfacial energy ΔG_V is the volume free energy given by the expression:

$$\Delta G_V = \frac{RT}{\Omega} ln\left(\frac{C}{C*}\right) \tag{3.32}$$

where C and C * represent solute concentration within the liquid alloy and equilibrium concentration, respectively $\frac{C}{C*}$ then becomes the driving force for the nucleation process.

The critical nucleus diameter d_c is given by

$$d_c = \frac{4\sigma\Omega}{RTln\left(\frac{C}{C*}\right)} \tag{3.33}$$

$C*$ is function of temperature and can be determined as the equilibrium composition from the liquidus line of the binary phase diagram. On the other hand, the supersaturation, C, that exists within the droplet in the initial stages for nucleation is difficult to determine experimentally and can also depend on the growth conditions. Gosele and coworkers[202] suggested that the composition in the liquid droplet can be correlated to the source partial pressure in the gas phase under steady state conditions. Assuming that this condition holds in the early stages, Equation 3.31 can be rewritten as

$$r_c^{min} = \frac{2\Omega^s\sigma^s}{k_B T ln\left(\frac{P_{Si}}{P_{Si}^{eq}}\right)} \tag{3.34}$$

where P is the pressure in the reference state, Ω^s is the molar volume of silicon, and σ^s is the surface energy of the droplet.

The driving force in equation 3.34(denominator on the right) comprises of two supersaturations: one in the liquid droplet that causes nucleation and another one in the vapor phase that maintains the spherical shape of the droplet. Again, equation 3.34 is difficult to use due to the unknown values for the reference state (P_{Si}) and the equilibrium partial pressure (P_{Si}^{eq}) . Equation 3.34 may be more appropriate during steady-state growth under precipitation kinetics limited conditions.

The interfacial energy of the droplet–crystal interface needs to be determined accurately for a reliable estimation of critical nuclei diameter. For a molten metal droplet in contact with a solid surface with an angle β (figure 3.6), the relation between the surface and interfacial energies at equilibrium is:

$$\gamma_{SV} = \gamma_{SL} + \gamma_{LV} cos\beta \tag{3.35}$$

where γ_{lv} is the liquid–vapor surface energy, γ_{sv} is the solid–vapor surface energy, γ_{sl} is the solid–liquid interfacial energy, which is used to calculate the critical nuclei size (equation 3.34).

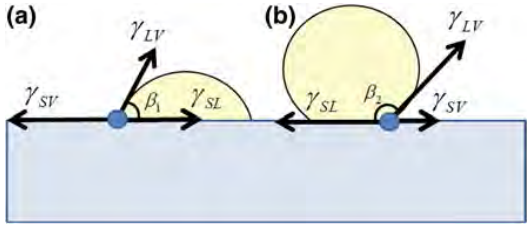


Figure 3.6 – *Liquid droplet on solid surface with equilibrium contact angle β1 < π/2 (a) and β2 > π/2 (b). The dot denotes the triple phase line. (Dubrovskii[199])*

3.2 The VS Growth Mode

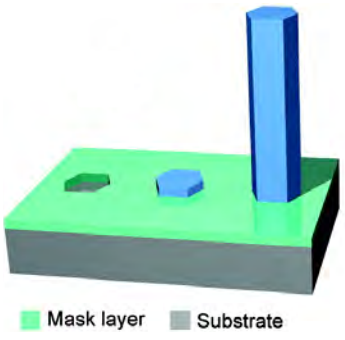


Figure 3.7 – *3D schematic of Vapor-Solid growth. (Mandl[203])*

Contrary to the VLS growth mode, the VS one shown in figure 3.7, does not involve a liquid metallic droplet for the nucleation. The nucleation stage proceeds with the formation of islands composed of high-index atomic planes[204] that undergo several shape transformations to form islands of nanowire morphology[205] . Since, the surface energy of the top facet is smaller than the side facets, it gathers higher quantities of group-III adatoms, which makes the vertical growth rate higher than the lateral one. However, for structures where higher radial growth is needed, for instance core-shell heterostructures, the growth temperature can be modulated in order to limit the migration of those adatoms to the top facet.

In the context of III-V nanowires, the VS growth mechanism is mostly implemented with Selective Area Epitaxy (SAE). In that case, a patterned oxide layer forces localized growth. GaAs[93] , InAs[206] and InGaAs[207] nanowires by Tomioka et al.[93,206,207] , InAsSb nanowires by Farrell et al.[208] GaN nanowires by Schiaber et al.[209] and recently InP nanowires by Gao et al.[210] are few examples of SAE.

3.3 The Crystalline Structure

In condensed matter, the crystalline structure corresponds to the periodic arrangement of atoms, ions or molecules in a crystalline material. This lead to the repetition of symmetric patterns along the principal crystal directions. The smallest pattern allowing full crystal reconstruction is called the unit cell of the structure. In the case of 2D growth of III-V materials, the crystalline structure is a cubic Zinc-Blend (ZB) one for most of them (except Nitrides) as presented in figure 3.8 (a and c). However, when the crystal dimensions are reduced, both cubic ZB and hexagonal Wurtzite (WZ) are reported [see figure 3.8(b and d)][200] . These two structures differ in the atom stacking sequence: in case of ZB, the bilayer stacking is ABCABC, whereas it is ABAB in WZ. In the ZB unit cell, group III atoms are located at each corner of the cube and at the center of each facet whereas four group V atoms have a tetrahedral geometry as shown in figure figure 3.8(a and c). On the other hand, in a WZ crystal, group III atoms are located at each corner and center of the top and bottom hexagons and 3 additional atoms are placed at the center of the cell; whereas group V atoms are directly located ontop of group III atoms in the c direction [figure 3.8 (b and d)].

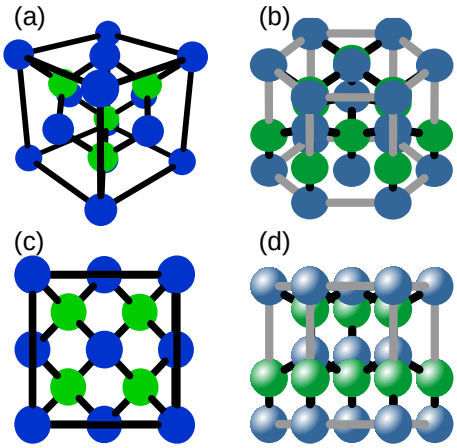


Figure 3.8 – *Crystalline Structures (a) and (c) : ZB and (b) and (d) WZ*

The reason of having a ZB or a WZ crystalline structure is related to the VLS growth mechanism and the position of the nuclei. Indeed, if the nuclei is located at the center of the interface between the droplet and the nanowire, it is favorable to growth a ZB bilayer; whereas if its position is at the triple phase boundary, also called the Triple Phase Line (TPL), WZ is favored (see figure 3.9[200]).

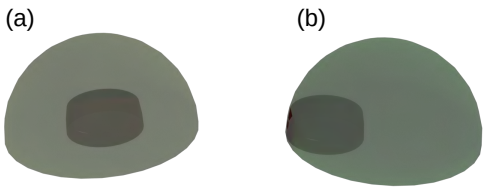


Figure 3.9 – *Different nucleation process. (a) non TPL nucleation and (b) TPL nucleation*

3.4 The Density Functional Theory

"The density functional theory (DFT) is a computational quantum mechanical modeling method used in physics, chemistry and materials science to investigate the electronic structure (principally the ground state) of many-body systems, in particular atoms, molecules, and the condensed phases".[211] This theory is based on the functional description of the electron density in a many-body electron system, in which nucleus are fixed (Born–Oppenheimer approximation) and generate a static external potential. Electrons are then described as wavefunctions influenced by this potential and are following the Schrödigner equation: $H\Psi = E\Psi$, where H is the Hamiltonian operator,Ψ is a set of solutions of H (eigen states) and E is the total energy. When considering multiple electron interactions with multiple nuclei, as is presented in figure 3.10, the Schrödigner equation becomes[212]:

$$[\ \frac{h^2}{2m}\sum_{i\,1}^{N}\nabla_i^2+\sum_{i\,1}^{N}V(r_i)+\sum_{i\,1}^{N}\sum_{j<i}^{N}U(r_i,r_j)\ ]\Psi = E\Psi \tag{3.36}$$

where m is the electron mass. The first term inside the bracket: $\frac{h^2}{2m}\sum_{i\,1}^{N}\nabla_i^2$ represents electron kinetic energy, the second term $\sum_{i1}^{N}V(r_i)$ is the interaction energy between each electron and the collection of atomic nuclei, and the final term $\sum_{i1}^{N}\sum_{j<i}^{N}U(r_i,r_j)$ is the interaction energy between different electrons. $\Psi = \Psi(r_1,.....,r_n)$ is the electronic wave function, which depends on the spatial coordinates of each electrons from 1 to N, and E is the ground state of electrons (spin neglected for simplicity). In our particular case, the ground state is independent of time and lead to a time-independent Schrödigner equation.

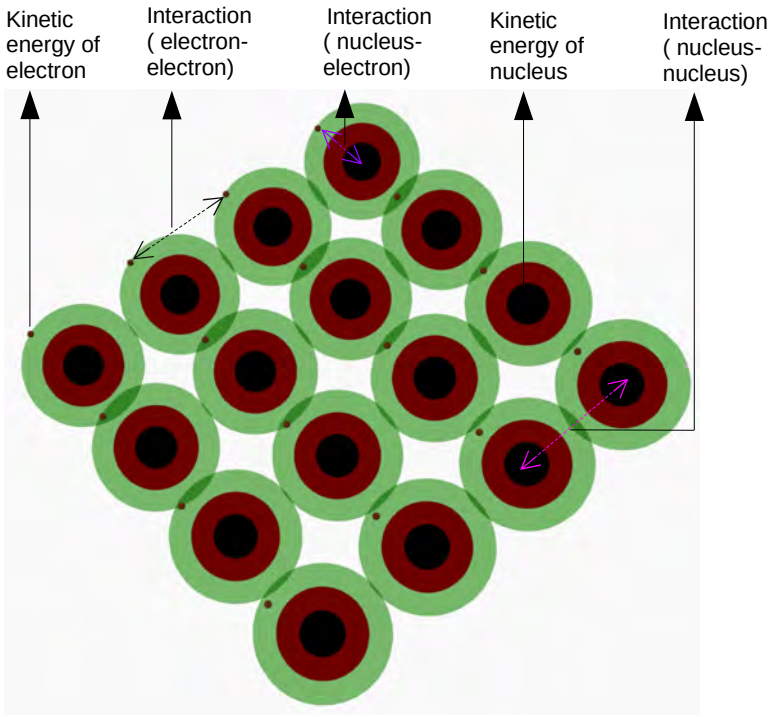


Figure 3.10 – *Many body interactions*

In this theory, the number of the electrons (N) is considerably larger than the number of the nuclei (M) since each nucleus has large number of electrons. As an example, a nanocluster with 100 Pt atoms requires more than 23,000 variables to define all wave functions. In addition, each individual electron wave function i.e $\Psi_i(r)$ cannot be retrieved unless individual electron wave function associated with all the other electrons are simultaneously considered. However, the problem can be simplified considering the probability matrix for these N electrons, of coordinates $r_1, ..., r_N$:

$$n(r) = 2\sum \Psi_i^*(r)\Psi(r) \tag{3.37}$$

where the term $\Psi_i^*(r)\Psi(r)$ is the probability that an electron with wave function $\Psi(r)$ is located in (r).Similarly, $\Psi_i^*(r)$ is the complex conjugate of $\Psi(r)$. The factor 2 comes from the spin contribution.

In this equation, the electron density $n(r)$, which is a very simple quantity: 3 variables, contains information about 3N coordinates given by the original Schrödigner equation. Since DFT is based on the electron density, it emerges as a powerful computational tool for solving the many body quantum mechanics problems.

The whole DFT field is based on two theorems given by Kohn and Sham in the mid 1960s. The first one states that "*The external potential (and hence the total energy), is a unique functional of the electron density*"[212]. This means that ground state density uniquely determines the potential, and thus all properties of the system (energy and wave function). Otherwise, the second theorem states that "*The functional that delivers the ground state energy of the system, gives the lowest energy if and only if the input density is the true ground state density*"[212]. This means that if true functional forms are known, one can find the relevant electron density by minimizing the energy of the function.

The energy function can be written as :

$$E[\{\Psi_i\}] = E_{known}\{\Psi_i\} + E_{XC}\{\Psi_i\} \tag{3.38}$$

The term $E_{known}\{\Psi_i\}$ can be further expressed as:

$$E_{known}[\{\Psi_i\}] = \frac{h^2}{m}\sum \int \Psi_i^* \nabla_i^2 \Psi d^3r + \int V(r)n(r)d^3r + \frac{e^2}{2}\int\int \frac{n(r)n(r')}{|r\,r'|}d^3r d^3r' + E_{ion} \tag{3.39}$$

Where the first term in the right $\frac{h^2}{m}\sum\int \Psi_i^*\nabla_i^2\Psi d^3r$ is the electron kinetic energies, the second term $\int V(r)n(r)d^3r$ is the coulomb interactions between electrons and nuclei, the third term $\frac{e^2}{2}\int\int \frac{n(r)n(r')}{|r\,r'|}d^3r d^3r'$ is the coulomb interactions between electrons and electrons and final term E_{ion} is the coulomb interactions between pairs of nuclei.

The term $E_{XC}\{\Psi_i\}$ of equation 3.38 is the exchange correlation functional and includes all the quantum mechanical effects that are not included by $E_{known}[\{\Psi_i\}]$.

Moreover, the Kohm-Sham equation is:

$$[\ \frac{h^2}{2m}\nabla_i^2 + V_H(r) + V_{XC}(r)\ ]\Psi_i(r) = \varepsilon_i\Psi_i \tag{3.40}$$

The difference between this 3.40 equation and 3.36 is that summation is not included in equation 3.40. This means that Kohm-Sham solutions are single-electron wave functions that depend on only three spatial variables: $\Psi_i(r)$. The left side of the Kohm-Sham equation (3.40) contain three different potentials: ∇, V_H and V_{XC}. The first term ∇ defines the interaction between an electron and the collection of atomic nuclei. The second term is the Hartee Potential, which describes the Coulomb repulsion between the electron being considered in one of the Kohn-Sham equation and the total electron density defined by all electrons in the problem . Its mathematical expression is :

$$V_H(r) = e^2 \int \frac{n(r')}{|r\,r'|} d^3r' \tag{3.41}$$

The last term V_{XC} is the "functional derivative" of the exchange energy and is expressed as:

$$V_{XC}(r) = \frac{\delta E_{XC}}{\delta n(r)} \tag{3.42}$$

At this point, the situation is bit odd, it is necessary to define the Hartee potential in order to get solutions of the Kohm-sham equations, but knowing the electron density is needed to get the Hartee potential and the electron density comes from the Kohn-Sham equations. The only way to break this loop is to follow an iterative process, which is shown in figure 3.11 considering a trial electron density at first.

The DFT is a powerful tool can that can be applied to many practical issues. It demonstrates high efficiency when the system is at equilibrium and can be used for description of defects, deformations, phonons and band structures in condensed matter. Furthermore, the total energy, binding energies of molecules and cohesive energies of solids can be predicted with DFT. The vibrational properties, vibrational spectra and even ionization potential can also be calculated with DFT. In the context of the Nanoelectronics, it can assist in understanding the surface preparations, the aging mechanisms, the oxide formations (including the functional oxides as SiO_2 on Si) and even having insights on defect formations in semiconductors.

In the context of this thesis, DFT simulations have been developed in order to describe surface preparations and nucleation mechanisms.

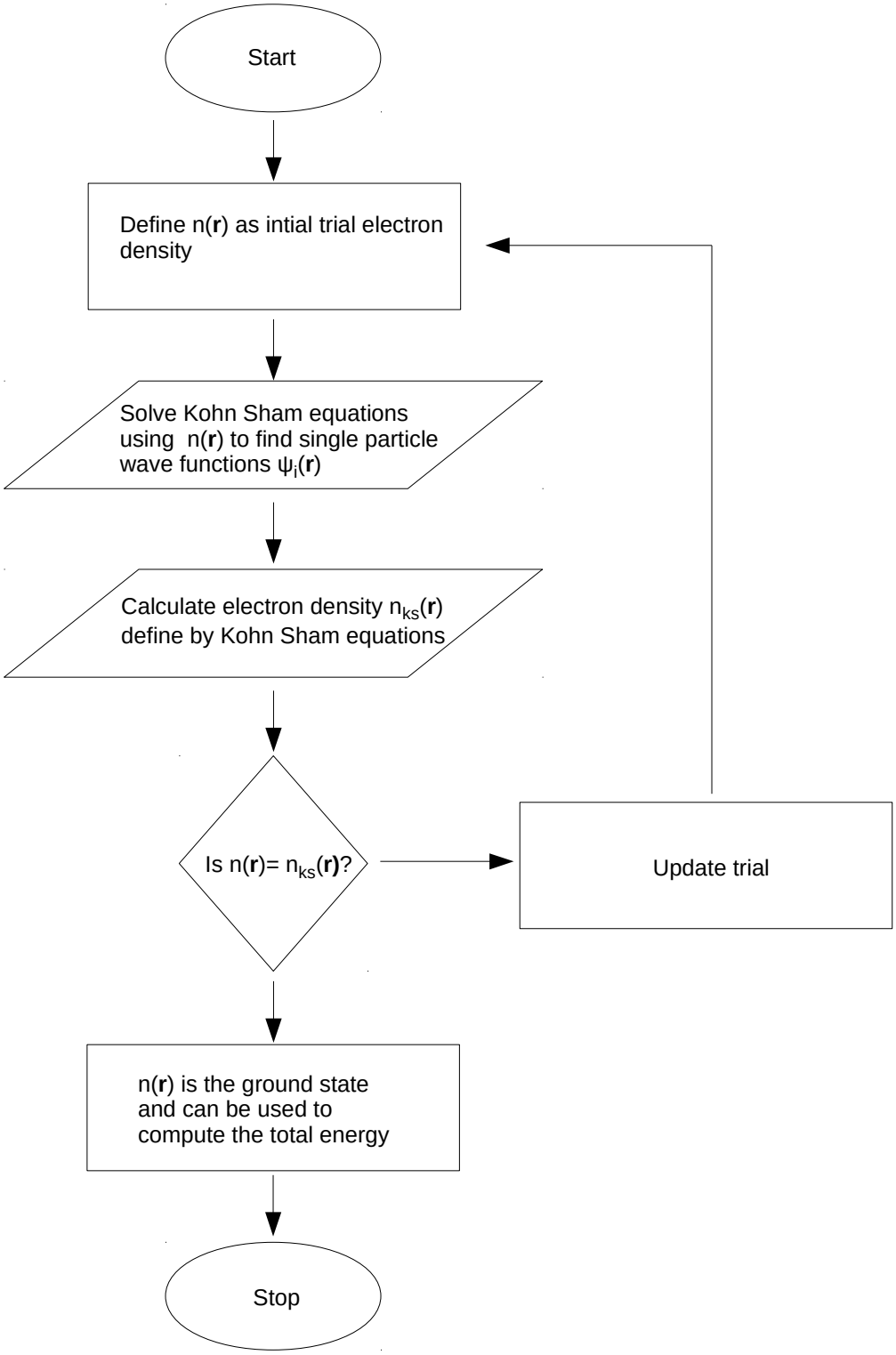


Figure 3.11 – *Flowchart to solve Kohn-Sham equations*

Chapter 4

Nanoelectronics with InAs Nanowires

The electronic technology, developed just after the second world war, had a groundbreaking impact on the globe and societies. This technology, now 70 years old, progressed from bulk electronics to microelectronics and now ultimately to nanoelectronics. The journey started with a 3 terminal device in 1947, whereas processors contain now billions of transistors. In the meantime, electronics reached major milestones such as the fabrication of Bipolar Junction Transistor (BJT), of Metal Oxide Semiconductor (MOS) and multi-gate field effect transistors (FET). Together with the change of the transistor architecture, multigate terminals, high-k materials, and new metallic gates were integrated to commercial devices.

In this framework, the chapter starts with a brief overview of these key historical achievements. First, the key devices: BJT, Field Effect Transistor (FET) and Complementary Metal Oxide Semiconductor (CMOS) are presented. Then, the scaling problems encountered for the 90 nm node will be explained, which lead a few years later to multigate architectures and the 10 nm node. In the meanwhile, integrated materials diversify a lot to improve device performances, which includes: stress engineering, high-k dielectric and the metallic gate.

The final section of this chapter presents our contribution to the field. Our goal is to develop a CMOS compatible bottom-up integration of InAs on Si(111) by Molecular Beam Epitaxy (MBE). First, the surface preparations that were developed during the thesis and allowed the growth of fully vertical and self-catalyzed InAs nanowires on Si(111) are discussed. Then a CMOS compatible process, that overcomes the Back-End-of-Line (BEOL) thermal limitations, was developed for growth of InAs nanowires on Si. The morphology and growth mechanisms of these nanowires will be discussed thanks to a complete statistical analysis. The chapter ends with some outlooks and conclusions for the field.

4.1 The Classical Electronics

4.1.1 The Bipolar Junction Transistor (BJT)

In 1947 three scientists from the Bell laboratory: John Bardeen, William Shockley and Walter Brattain unveiled the first point contact Germanium transistor. Three years later, William Shockley developed a current controlled switch with three terminals: a base, a collector and an emitter, known as the BJT (figure 4.1). In this transistor, a lightly doped base is sandwiched between oppositely doped collector (moderately doped) and emitter (highly doped), allowing thus two different architectures of BJT: npn and pnp. As suggested by the name, in a npn BJT, carriers are electrons that flow from highly doped n type emitter to moderately doped n type collector when a positive bias is applied on the lightly doped p-type base, which separates those two terminals. In a pnp BJT, the architecture is the opposite. Compared to the vacuum tubes technology of that time, these new devices were already smaller, power efficient and more reliable. In 1958 Jack Kibley from Texas Instruments built the first Integrated Circuit (IC) using two BJT, connected on a single piece of Silicon, marking the start of silicon era. Despite several promises: high transconductance, high speed, high maximum frequency and high gain; the integration of BJT into IC did not skyrocket due to the high electrostatic power dissipation of the current controlled switches. Note here that the static power dissipation of a transistor is the power that is consumed when the device is in the sleep mode. In opposite, dynamic power dissipation refers to the additional power consumed when the device is in operation. Higher amount of power dissipation means that the device will generate more heat and, consequently it is impossible to integrate a large number of BJTs onto the same IC.

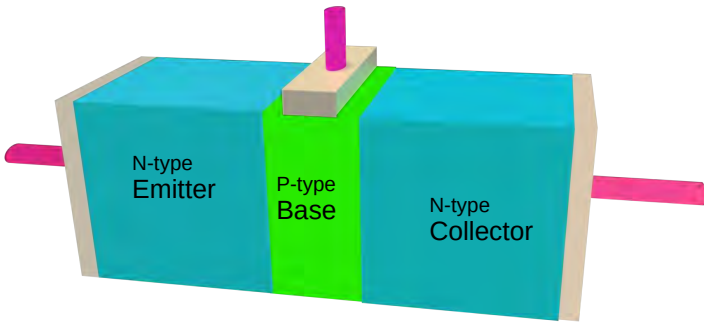


Figure 4.1 – *Bipolar Junction Transistor*

4.1.2 The Field Effect Transistor (FET)

Another major breakthrough was reported by Texas Instruments in 1959 when the first insulated gate FET (also known as MOSFET) was developed. A FET is a voltage controlled switch in which a bias voltage from one of its terminal (Gate) is used to control the flow of current between the two other terminals (Source and Drain) through a semiconducting channel. A MOSFET can either be a NMOS (figure 4.2) or a PMOS (2 complementary architectures) depending of the carrier that flows during operation. If the semiconducting channel conducts electrons from the source to the drain under a positive gate bias, the device is a NMOS (figure 4.2). In this device, the semiconducting

channel is sandwiched between two highly n-doped source and drain; and lies on top of a p-type substrate. Right above the channel, an insulating oxide separates it from the gate electrode. The high doping levels (n+) of both source and drain ensures minimum resistance to the current flow. In addition, the identical doping of source and drain makes them interchangeable.

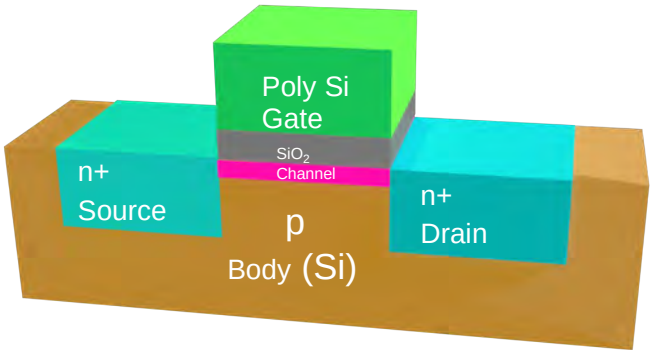


Figure 4.2 – *Scheme of a Field Effect Transistor (NMOS)*

Since MOS devices are voltage controlled, the current that flows in the channel is determined by the gate bias (V_{gs}). When the gate voltage is sufficient (positive in NMOS), the positive charges are collected in the gate, which will repel minority carriers (holes) in the p-type substrate, leaving path for majority carriers (electrons) and thus creating a depletion region. If V_{gs} is increased furthermore, lot of electrons are attracted towards the semiconductor/insulator gate interface, which generates an inversion region. If the drain-to-body potential is higher than the source-to-body potential, the depletion region increases as reverse biasing is increased. Finally, when drain-to-source is positively biased, electrons can flow through this conducting channel from source to drain giving a current (I_d).

A famous device was built using this architecture in 1971 by Intel: the Intel-4004 chip, a 4 bit central processing unit (CPU) with dimensions of 0.11x0.15 inch containing 2300 MOS. One year later, Intel announced a 8 bit processor by doubling the number of transistors: the Intel 8008. Even if the NMOS technology offers many advantages: cheap, small size, high packing density; the static power dissipation in a NMOS is high compared to a CMOS (the next industry standard), which became a serious issue in the 1980s.

4.1.3 The Complementary Metal Oxide Semi-Conductor (CMOS)

It is in 1963 that C. T. Sah and Frank Wanlass[213] of the Fairchild R&D Laboratory reported the possibility to have a close to zero power device, in standby mode, by using two complementary channel transistors: NMOS and PMOS; the complementary symmetry circuit configuration was born. The biggest advantage of this configuration is that there is nearly zero static power dissipation which led the industry to take it as a standard few years later and for several decades.

To this point, it is clear that the important parameters that drove microelectronics are: lower power consumption, high packaging densities, high speed and high performance to cost ratio. In the following years, the CMOS technology improved scaling, which helped the miniaturization. The scaling was inspired by a famous statement from Gorden Moore in 1965, the co-founder of Intel,

also known as the "Moore's Law". It states that the number of transistors per square inch should double in every 24 months. The primary goals of scaling are: (i) the improvement in the transistor density and operating frequency, and (ii) the reduction of power dissipation. The scaling reduces the transistor dimensions including the gate length and width, the oxide thickness and the depletion layer. The first scaling table was provided by Dennard et al.[214] in 1974, which is known as the constant electric field scaling and that boosted the CMOS technology up to the 90 nm node. Note that the assigned number for a node refers to the channel length. In general, there are two types of scaling: the constant field scaling and the constant voltage scaling. Table 4.1 summarizes the effects of these two types of scaling on some of the important physical parameters.

SN	Physical Parameter	Symbol	Constant Field Scaling	Constant Voltage Scaling
1	Gate Length	L	λ^{-1}	λ^{-1}
2	Gate Width	W	λ^{-1}	λ^{-1}
3	Electric Field	E	1	λ
4	Junction Depth	x_j	λ^{-1}	λ^{-1}
5	Gate Oxide Thickness	t_{ox}	λ^{-1}	λ^{-1}
6	Substrate Doping Density	N_A	λ	λ^2
7	Gate Oxide Capacitance	C_{OX}	λ	λ
8	Gate Capacitance	C_{gate}	λ^{-1}	λ^{-1}
9	Threshold Voltage	V_{Th}	λ^{-1}	1
10	Drain-Source Voltage	V_{DS}	λ^{-1}	1
11	Drain-Source Current	I_{DS}	λ^{-1}	λ
12	Power	P	λ^{-2}	λ
13	Transit Time	t_{tr}	λ^{-1}	λ^2
14	Transit Frequency	f_t	λ	λ^{-2}
15	Power Dissipation	P	λ^{-2}	λ
16	Power-Delay	$P\Delta t$	λ^{-3}	λ^{-1}

Table 4.1 – *The effect of the constant field and the constant voltage scaling. (Khanna[17])*

4.1.3.1 The Constant Field Scaling

For the constant field scaling, both the horizontal and the vertical dimensions of the transistor are scaled down by a factor λ. Hence, the electric field, which is the ratio between voltage and distance, scales down by λ. Since, the length (L), width (W), oxide-thickness (t_{ox}), the input voltage (V_{DD}) and the threshold voltage (V_{th}) scales down by λ, the doping concentration needs to be scaled-up by λso that the electric field in the transistor remains constant. Consequently, this is limited by the higher doping level achievable for substrates:$10^{-18}cm^{-1}$. This limit comes from the substrate fabrication and the maximum dopant solubility in silicon, which is the maximum impurity concentration that can be introduced at a given temperature before it starts to precipitate out. The major drawback of this scaling is reached when the driving voltage (V_{dd}) should be below $1V$, since noise in the system starts to be important: lower V_{dd} requires larger doping concentration to maintain a good Signal to Noise Ratio (SNR).

4.1.3.2 The Constant Voltage Scaling

As the name suggests V_{dd} is kept constant in constant voltage scaling. The dimensions that are perpendicular to the surface are scaled down by a factor λ. This results in an increase of the drain current (I_{ds}) by a factor λ; the gate delay decreases by λ^2 , the power density increases by λ^3, and the doping concentration scales up by λ^2. The biggest advantage of this approach is that low threshold issues are not appearing; but since the supply voltage is not scalable anymore, the power density increases by a factor λ^3, which lead to heat dissipation problems. In addition, the aggressive scaling of the doping concentration by λ^2 forces the depletion region to be scaled down by λ.

4.2 The Short Channel Effects

When the MOSFET channel length is comparable to the depletion width of the source and drain, it is named a "short channel". This shrinking of the channel increases the vertical electric field (Ey) in the channel region, making it no negligible anymore. As a consequence, the MOSFET behavior deviates from a long channel one and the so-called "short channel effects" appears. Moreover, the channel experiences a 2D potential distribution, which dependents on the transverse electric field (Ex) and the bias applied on the back surface. Because of this, the threshold voltage becomes dependent of the channel length and of the bias voltage. Seven kinds of short channel effect are reported below:

1. **Reduction in the threshold voltage**: In a long channel MOSFET, the channel is fully controlled by the gate and the depleting regions from the gate and the source are fully neglected. Hence, the potential profile is 1D. However, for short channel transistors, the depletion region from the source and gate can not be neglected anymore. More importantly, the potential profile becomes 2D. As a result, a charge sharing takes place between the 4 terminals (the source, the gate , the drain and the substrate) in contrast to long channel transistors. This lowers the gate threshold voltage, which is compensated by an offset.

2. **The Drain Induced Barrier Lowering (DIBL):** For short channels, the increase of the drain voltage (V_d) widens the drain depletion region and eventually reduces the potential barrier. As a consequence, the threshold voltage decreases, which leads to higher leakage currents since the channel control is lowered.

3. **The Carrier Velocity Saturation**: In short channels, since the longitudinal electric field (E_x) increases and becomes large, the carrier velocity is no more proportional to the vertical electric field (E_y). This results in a linear increase of the saturation current (I_{DS}) with respect to $V_{GS} - V_{Th}$ instead of the quadratic one, which reduces the transconductance.

4. **The Surface Scattering:** Similarly, an increase in E_x makes the surface mobility of carriers field dependent. Considering the fact that the carrier transport in a MOSFET should be confined within the inversion layer beneath the gate oxide, electrons experience difficulties to move parallel to the interface as they suffer collisions. This degrades the carrier mobility.

5. **The Punch-through:** When the drain bias reaches to an extreme level of DIBL, the drain depletion region extends towards the source and the two depletion regions can merge. In this case, the gate has no more control over the channel.

6. **The Impact Ionization:** In a short channel, since carriers experience a high electric field close to the drain, they get a significant amount of energy, which can lead to ionization impacts and creation electron-hole pairs. Furthermore, the multiple ionization impacts lead to an avalanche of free carrier. The drain attracts electrons, while holes move towards the substrate, which lead to a voltage drop in the substrate. This creates a scenario where the N+ source - P substrate - N+ drain acts as a NPN transistor. Since, the voltage drop in the substrate makes source-to-substrate forward biased, electrons can flow from source to substrate rather than from source to drain. Furthermore, these electrons in the substrate region can move towards the drain and make things worst by further creating electron-hole pairs.

7. **The Hot Carriers Effects:** The carriers in a short channel (either electrons or holes) acquire very high kinetic energies, because of the high electric field, and are called "hot carriers". They can migrate to the forbidden areas of the transistors such as the gate dielectric and the substrate, which causes shift in the threshold voltage and a degradation of the transconductance. This effect is more serious for N-type MOSFET since electrons have higher mobilities compared to holes.

These short channel effects confirm further the scaling limitations beyond 100 nm and led to new approaches such as strain engineering, high k dielectric, metal gate and multi-gate architectures, which is presented in the following sections.

4.3 The semi-classical Electronics

4.3.1 The High-K Dielectrics

The gate oxide thickness is one of the physical parameters that was continuously scaled down during the miniaturization processes as presented in table 4.1. However, for oxide thicknesses below 3 nm, the quantum mechanical tunneling of electrons from the gate to the underlying silicon starts to become prominent. These quantum mechanical effects increase the gate leakage current which is highly undesirable. The thickness of the gate oxide t_{ox} can be mathematically expressed as :

$$t_{ox} = \frac{E_{ox}}{C_{ox}} \tag{4.1}$$

Where E_{ox} is the electric field in the oxide and $C_{ox}$is the capacitance of the oxide. Considering a parallel plate configuration, it can be expressed as :

$$C_{ox} = k_{ox}\frac{\varepsilon_0 A}{t_{ox}} \tag{4.2}$$

where k_{ox} is the relative dielectric constant of the oxide, ε_0 is the vacuum permittivity and A is the capacitor area. From equation 4.1 and 4.2, it is clear that if the oxide material has a higher dielectric constant, the gate leakage currents can be minimized. The CMOS industry quickly adopted this concept and $Hf0_2$, which has the dielectric constant of 25 (6 times higher than SiO_2), became the new standard starting with Intel's 45 nm node.

4.3.2 The Metallic Gates

The metallic gates were commonly used in the transistor architectures when the operating voltage was in the $3-5$ V range (before 1980s); but the necessity of lower threshold voltage during CMOS downscaling made industry switch to the poly-silicon (poly-Si) gates. Indeed, since the underneath material (Si) is the same, lower threshold voltage for both NMOS and PMOS are easier to achieve. Another advantage of poly-Si is that it can withstand very high temperature compared to metallic gates. For example, the melting point of poly-Si is 1100 °C while it is only 660 °C for Al. Unfortunately, poly-Si is a semiconductor, so it depletes in the presence of high electric field. The extreme level of CMOS downscaling gave rise to a finite depletion layer inside poly-Si. This was mitigated either by reducing the oxide thickness t_{ox} or by increasing the doping concentration $(N_A or N_D)$. However, both of these parameter reached their limit; 1.5 nm for t_{ox} , 10^{-20} $cm^{-3}$for N-type doping and 10^{-19} $cm^{-3}$for P-type doping. The only solution to overcome these limitations and to limit leakage currents is then to use again metallic gates. This issue was addressed by Intel for the 45 nm node, by using the metal gate (TiN) instead of poly-Si. Finally, a metallic gate allows also the use of a high-k dielectric and eliminates the depletion effect in poly-Si.

4.3.3 The Strain Engineering

The carrier mobility refers to the velocity at which the carriers (electrons or holes) travel in the presence of an electric field. The transistor performances are directly linked to this mobility since the transistor commutation speed improves when carriers travel with higher velocities. Mathematically, the carrier mobility is defined as the ratio between the drift velocity (v_d) and the electric field (E) :

$$\mu = \frac{v_d}{E} \tag{4.3}$$

The idea behind strain engineering is to boost the carrier mobility using a strained silicon channel. If we now consider the Drude equation :

$$\mu = \frac{q\tau}{m^*} \tag{4.4}$$

where q is the charge, τ is the mean scattering time and $m*$ is the effective carrier mass. The two terms:τ and $m*$ from equation 4.4 can be modified when strain is introduced in the system. Indeed, when the silicon crystal is subjected to an uniaxial strain, the crystal lattice is altered, which leads to a modification of the band structure, the density of states and the carriers effective mass. This depends on the surface orientation and the channel direction.

When a thin Si layer is grown on a thick SiGe one, the lattice constant of the underlying crystal is preserved, which produces bi-axial strain in Si. The electron mobility is enhanced when a tensile strain is applied, whereas it is the opposite for holes.

The strain engineering can be carried out by the following ways :

1. **Wafer bending:** The wafers are subjected to a mechanical strain via one plate placed above. The amount of strain produced on the surface depends on the sample thickness and the radius of curvature. In this case, there are three strain components: σ_{xx} ,σ_{yy} and σ_{zz}.

2. **Nitride strain liner:** When tensile nitride films are deposited on the source and drain, a tensile strain is developed along the channel, which enhances the electron mobility. This technique is commonly used to improve CMOS performances. Similarly, a compressive strain is obtained with a deposition on the source and drain sidewalls. The key parameters for this technology are the strain level, the transistor spacer width, the gate height and the length of source, drain and gate.

3. **Embedding SiGe and SiC on Source and Drain:** When embedded on source and drain, SiGe generates a compressive strain in the silicon, which improve the hole mobility. Similarly, the integration of SiC boosts the electron mobility of NMOS, since a tensile strain is induced in that case.

4. **Local strain from the gate electrode:** In the multi-gate devices, the tensile strain can be engineered directly from the gates, using highly tensile metals. Furthermore, this approach is not layout dependent and can be implemented on long channels. Unfortunately, this method cannot improve holes mobility due to the lack of possible compressive metals. Finally, if the metal gate experiences high temperatures, it can squeeze them from both sides in multi-gate system due to different thermal expansion coefficients.

5. **Strain from the substrate or strained Si on Insulator:** In the former case, the idea is to generate strain from the substrate by growing a thin Si layer on a relaxed SiGe buffer layer. In the latter case, strained Si on Insulator (sSOI) is obtained by using wafer bonding techniques, which allows to combine different materials without creating crystalline defects and misfit dislocations. The growth of the SiGe bulk layer is also avoided.

4.3.4 The Silicon On Insulator and the Multi Gate Architectures

The major challenge that the CMOS industry faced during the down scaling is the loss of channel control when reaching nanoscale (especially below 28 nm for the gate length). This led to a serious increase of the transistor leakage currents. This has been overcome thanks to two major innovations: the Silicon On Insulator (SOI) technology and the multi-gate architecture (figure 4.3).

The motive behind the SOI technology is to improve the device performances by removing some unwanted silicon material responsible of parasitic effects and replace it by a buried oxide layer (under the channel). This new architecture improves the overall device performances compared

to bulk MOSFET, and allows high density, low power consumption and lower cross talk between transistors.

On the other hand, the multigate architecture objective is to improve the gate control on the channel by increasing the electrostatic confinement. In 1980s, it was already reported[216] that a two gates system has better performances than a single gate one. This triggered a lot or research interest on multigate transistors and resulted in single, double, triple and surrounding gate architectures as presented in figure 4.3 (next page). In the latter version, the channel of the transistor is completely surrounded by the gate, which lead to the better $\frac{Ion}{Ioff}$ ratio. This configuration, also called the Gate-All-Around (GAA or cylindrical FET) architecture, can either be implemented horizontally or vertically, which hold promises for developing a 3D transistor. In this context, nanowires could represent an ideal geometry for the next generation of transistors. Indeed, in 2011, the FinFET technology was implemented by Intel in its 28 nm node, in which the drain-source current is increased thanks to multiple channel placed in parallel and controlled by a single gate[217]. At present (2018), the latest processor for the mobile handsets: the Qualcomm Snapdragon 845 chipset is based on a 10 nm FinFET manufacturing process, while Apple's A12 processor will use 7nm chipset. In future, the FinFET architecture could be advantageously replaces by parallel vertical nanowires as suggested by the International Technology Roadmap for Semiconductors (ITRS).

4.3.4.1 Physics Behind multi gate architectures

The figure 4.4 presents the electric field in a multigate system at the position (x,y,z) inside the channel. W_{si} represents the width of the channel and T_{si} is the thickness.

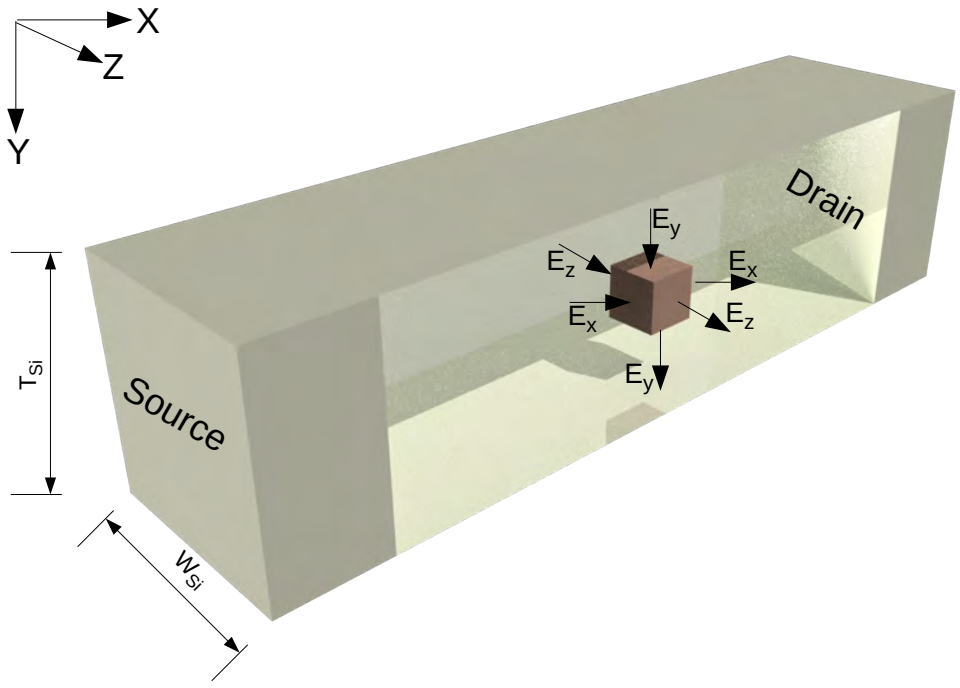


Figure 4.4 – *Electrical field in multi-gate system*[215]

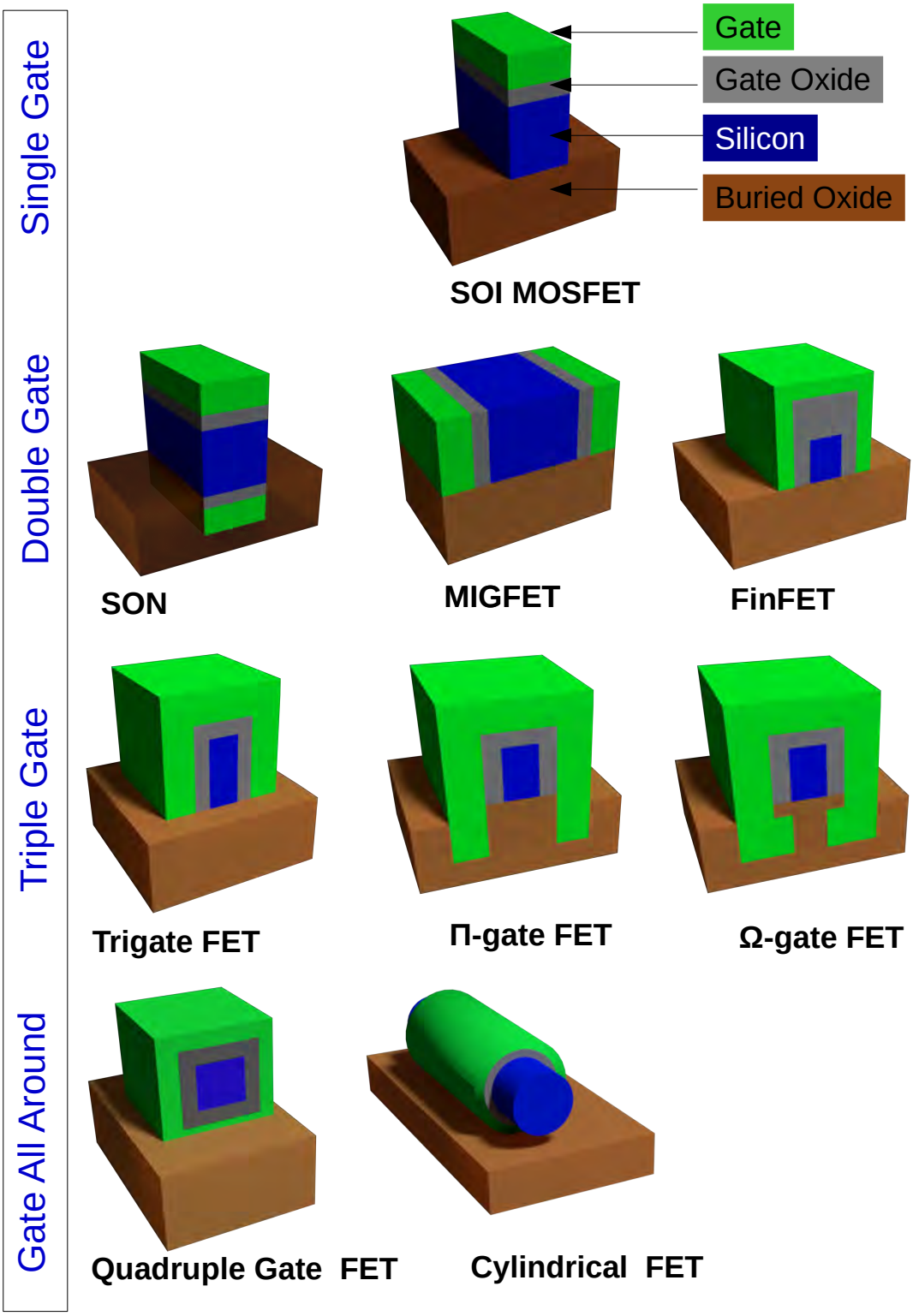


Figure 4.3 – *Different Gate Structures. This particular case of SOI can be adapted to the standard CMOS technology. (Adapted from Colinge*[215]*)*

In this system, the Poisson equation can be written as:

$$\frac{d^2\Phi(x,y,z)}{dx^2}+\frac{d^2\Phi(x,y,z)}{dy^2}+\frac{d^2\Phi(x,y,z)}{dz^2}=\frac{qN_a}{\varepsilon_{si}} \tag{4.5}$$

where is q is the total charge, N_a is the channel doping concentration and ε_{si} is the dielectric constant of silicon.

In terms of electric field, equation 4.5 can be rewritten as:

$$\frac{dE_x(x,y,z)}{dx}+\frac{dE_y(x,y,z)}{dy}+\frac{dE_z(x,y,z)}{dz}=C \tag{4.6}$$

where C is a constant.

In this 4.6 equation, if one of the left term is increases, the two other one need to compensate as the total is constant. In the geometry presented in figure 4.4, the x component of the electric field- $E_x(x,y,z)$ corresponds to the drain electric field, which is a source of unwanted short channel effects. This drain influence can be decreased by either increasing the channel length or by increasing the channel gate control. For short channels, this control can be improved by increasing the doping concentration or by increasing the gate number. Since, the doping level has a upper limit, the multigate architecture is the only viable solution. From figure 4.4, it is thus clear that top and bottom gates can control $\frac{dE_y(x,y,z)}{dy}$ and that $\frac{dE_z(x,y,z)}{dz}$ can be optimized by adding two lateral gates in the z direction. Compared to the single gate system of a conventional planar MOSFET, these additional gates will lead to a better electrostatic control of the channel.

Solving the 4.6 equation, solutions can be written as[215] :

$$\varphi(x)=\varphi_0 e^{(\pm\frac{x}{\lambda_i})} \tag{4.7}$$

where λ_i is a parameter that represents the spread of the electric potential in the x direction. λ_i is called the "natural length" of the device. It depends on the gate oxide thickness and the silicon film thickness. The thinner the gate oxide and/or the silicon film, the smaller the natural length and, hence, the influence of the drain electric field on the channel region. Numerical simulations show that the effective gate length of a MOS device must be larger than 5 to 10 times the natural length to avoid short-channel effects.

Table 4.2 reports the natural length of a multigate system as a function of the transistor architecture.

Number of gates	Natural Length
Single Gate	$\lambda_1=\sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{si}t_{ox}}$
Double gate	$\lambda_2=\sqrt{\frac{\varepsilon_{si}}{2\varepsilon_{ox}}t_{si}t_{ox}}$
Quadruple Gate (Square geometry)	$\lambda_4=\sqrt{\frac{\varepsilon_{si}}{4\varepsilon_{ox}}t_{si}t_{ox}}$
Surrounding Gate (Circular Geometry)	$\lambda_0=\sqrt{\frac{2\varepsilon_{si}t_{si}^2 ln(1+\frac{2t_{ox}}{\varepsilon_{si}})+\varepsilon_{ox}t_{si}^2}{16\varepsilon_{ox}}}$

Table 4.2 – *Effective Effective gate length of a multigate system*[215]

Otherwise, it is possible to introduce the concept of Equivalent Number of Gates (ENG), which corresponds to the number of gates around the channel assuming a square cross section. From the natural length mathematical expression, it represents the integer dividing $\frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{si} t_{ox}$. From table 4.2, it is apparent that the possible ways to avoid short channel effects are: to decrease the gate oxide thickness (t_{ox}), to decrease the silicon film thickness (t_{si}), to increase ε_{si} by using a high-k dielectric and to increase the gate number. In very small devices, the reduction of the oxide thickness below 1,5 nm causes gate tunneling current problems. Using multi-gate devices, it is possible to trade a thin gate oxide for thin silicon film/fin thinning since λ is proportional to $t_{si} t_{ox}$.

In summary, the GAA architecture is the one providing the better electrostatic control and thus is the most optimized configuration. Furthermore, corner effects, which appear in the multigate architecture, are ruled out if the material is intrinsic. The nanowire geometry fits perfectly this concept, and the nanowire nanoelectronics will be discussed in the next section.

4.4 The High Mobility Nanowires

During the 2015 ITRS meeting, semiconducting nanowires were presented as one of the most promising building blocks for the next generation of CMOS transistors. The report summarizes their advantages as: a large choice of materials is available (III-V, II-V, Si , Ge etc), the possibility to have 1D ballistic transport, and the opportunity to build a 3D transistors using a vertical GAA-FET architecture. Furthermore, the report emphasizes that n-type FET exhibits excellent electron mobilities for III-V compound semiconductors.

The table 4.3 summarizes the basic intrinsic properties of potential interesting channel materials. If the electron mobility is considered, low bandgap III-V materials such as InAs and InSb are very interesting, since it is respectively 28 and 55 times higher than in Si. This means that electrons will travel faster in NMOS if the channel can be replaced with these materials. Similarly, GaSb and Ge are promising for PMOS considering their hole mobilities. Furthermore, the ternary alloys: $InAs_{1-x}Sb_x$ and $GaAs_{1-x}Sb_x$, whose properties depend on the (x) composition are even more interesting. However, their integration in the CMOS platform (i.e. on Si) faces two major bottlenecks. First, the lattice mismatch with Si makes the integration very challenging: it is 11.5 % for InAs, 12.2 % for GaSb and 19.3 % for InSb. Secondly, the growth process should be gold-free, as gold creates detrimental mid-gap defect levels in silicon.

Furthermore, the growth should be technologically controlled in order to have uniform, fully vertical thin nanowires on Si, if the ultimate goal is the 3D transistor.

	Si	Ge	InP	GaAs	GaSb	InAs	InSb
Electron Mobility (cm^2/v.s)	1400	3900	5400	8500	3000	40000	77000
Hole Mobility (cm^2/v.s)	450	1900	200	400	1000	500	850
Bandgap (eV)	1.12	0.66	1.34	1.42	0.726	0.35	0.17
Lattice Constant (Å)	5.431	5.658	5.869	5.653	6.095	6.058	6.479
Dielectric Constant	11.7	16.2	12.5	12.9	15.7	15.2	16.8

Table 4.3 – *High carrier mobility Materials*

Due to their unique properties, the growth and characterization of nanowire, based on these material families, were widely reported in the past decade. Several transistor geometries were studied including GAA[207] and Tunneling FET (TFET)[218] and different materials considered: InAs[206], InGaAs[207] and heterostrucures like InP/InAs[219], GaSb/InAs[220]. Nevertheless, CMOS compatibility as never been reported since either the growth is not on silicon, or is not gold-free or is above the Back-End-of-Line (BEOL) temperature limit.[221,222] Closest results to full CMOS compatibility, were presented by the group of professor Fukui from the Hokkaido University, (Sapparo in Japan) and based on the GAA architecture with InAs[223] and InGaAs nanowires[207] and on a TFET architecture with InAs nanowires[218]. The key parameter for these successful studies is the surface preparation as it will be explained in the following sections.

In their groundbreaking paper in 2008, Tomioka et al. (group of professor Fukui), using a MOVPE system, demonstrated the integration of fully vertical and self-catalyzed InAs nanowire on Si(111)[206] and reported the first nanowire based 3D transistor[223,224]. In the following years, other research groups[203,225–233] using MOVPE reproduced these results[206,207,223,234] and achieved high vertical yield (>85%) in the patterned substrates with ease. On the contrary, reports from MBE groups[235–238] highlighted significant difficulties to match these results. If these difficulties are supposedly due to the presence of native oxide and large lattice mismatches; one can also suppose that growth environment and surface preparation are crucial. Indeed, the surface reconstruction in a MOVPE chamber, due to the H_2 carrier gas and the high temperature in-situ annealing under As_2, seems to be of firm importance in the process.

There are common agreements regarding the vertical and self-catalyzed growth of III-V nanowires on silicon. Fontcuberta et al.[89] reported the importance of the silicon oxide thickness in the case of GaAs nanowires and Tomioka et al.[206] emphasized the necessity of a complete native oxide removal for InAs NW nucleation and the creation of a Si(111)B surface before growth. In the latter case, a pre-growth high temperature annealing in the presence of H_2 and As_2 is performed in order to create a Si(111)B surface. This high temperature annealing seems to be dependent of the growth system from 950 °C for Tomioka et al.[206]down to 630 °C for Wang et al.[239]. The reported temperatures are always above 500°C[203,225–233]. Hence, one can conclude that the surface preparation is one of the crucial steps that need to be addressed and fully understood in order to achieve a complete CMOS compatibility.

Moreover, one should note that there are four (111) directions on a (111) substrate: one vertical and three tilted (angle of 19.2° with respect to the substrate and 120° between them). Since nanowires are growing in the [111]B direction and silicon is non polar, the four growth directions are possible (in opposition with a polar III-V substrate having one [111]B and three [111]A directions). It is thus mandatory to create a B-type polarity on the silicon substrate to achieve fully vertical growth.

4.5 My Contribution

These contrasting results between InAs growth by MBE[235–238] and MOVPE[203, 206, 225–233] are quite surprising. One difference between the two system is the presence a H_2 carrier gas in MOVPE. In order to address this, an in-situ hydrogen plasma cell (RF-sourced) was integrated on the preparation chamber of our MBE system. This allowed us to study and understand the influence of the H_2 environment during the surface treatment process that takes place before growth. Details on instrumentation and working principle of the H_2 treatment are given in Appendix A.

4.5.1 The Initial Growths

In order to study the influence of the surface preparation, few growths with fixed epitaxial growth parameters were carried out in order to probe the different surface treatments. Only one parameter was probed, keeping surface treatment and growth parameters constant. The parameters that were probed are: (i) the influence of the degassing temperature in the H_2 environment, (ii) the influence of the H_2 flux during degassing and (iii) the influence of the arsenic annealing temperature in the growth reactor just before nanowires growth. Note that, the optimized parameter was chosen. This initial study is reported in the next three subsections.

4.5.1.1 The Experimental Description

The nanowires are grown on commercially available 2 inch NID Si(111) wafers from Siltronix in a solid-source MBE system (RIBER-MBE412). Once the native oxide is removed with the help of hydrofluoric acid (HF 5%), substrates are immediately loaded into the MBE chamber. The degassing of these wafers is carried out either a degassing temperature [200 °C / 650 °C (only varied while probing the influence of degassing temperature during H_2 treatment)] for 1 hour under an Hydrogen plasma flux of [0.5 / 1 / 2 / 3 / 5 sccm (RF source and Power = 250 Watts); (only varied while probing the influence of the amount of H2 flux during plasma treatment)]. Next, the substrates are loaded into the growth chamber where they are directly heated up to the annealing temperature [650 °C / 500 °C / 450 °C (only varied while probing the influence of the high temperature arsenic annealing temperature] under an arsenic flux of $2x10^{-7}$ Torr for 20 minutes. After this step, the substrates were cooled down to the growth temperature (410 °C). Finally, the nanowire growth is initiated by opening the indium shutter for 1 hour, with and indium flux of $3.1x10^{-8}$ Torr and and arsenic flux of either 1.2 / $2.1x10^{-5}$ Torr. Note that an In flux of $3.1x10^{-8}$ Torr corresponds to growth rate of 0.02 monolayer/sec on GaAs and an As flux of $2.4x10^{-5}$ Torr corresponds to a growth rate of 1 monolayer/sec on GaAs. The specific and any changes in the growth parameter will be mentioned whenever necessary. After growth, nanowires are cooled down to 200 °C using the same arsenic flux. The nanowires were characterized by Scanning Electron Microscopy (SEM) (FEIAztec600i).

4.5.1.2 Influence of the degassing temperature during Hydrogen treatment

Figure 4.5 presents as-grown SEM images of samples having either a low [4.5(a) 200 °C in green box] or a high [4.5(b) 650 °C in red box] degassing temperature during the H_2 plasma. The scatter plots below the SEM images were constructed taking at least 150 nanowires (if needed multiple images from the same sample were considered). Each point of the plot corresponds to a wire with its unique value of length (Y-axis) and diameter (X-axis). The violin plot represents the probability distribution (X-axis) of a wire to have a length L (Y-axis) and the additional three lines represents the 1^{st} quartile, the median and the 3^{rd} quartile respectively. The plot is centered on the mean diameter (X-axis). Nanowires are fully vertical in both the cases, which confirms the full removal of the native oxide. Diameter is lower and aspect ratio is higher for the low temperature plasma treatment [Figure 4.5(a)], which suggests different surface reconstructions. For this reasons, the degassing temperature is fixed to 200 °C in the following of this chapter.

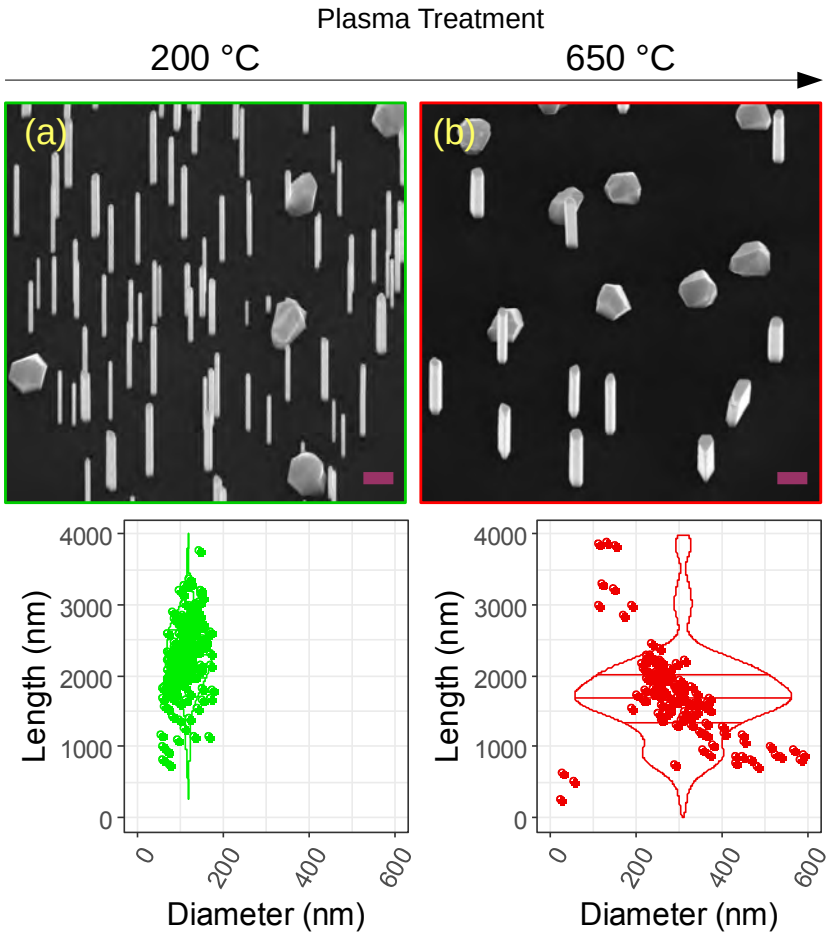


Figure 4.5 – *Plasma treatment at low and high temperature. The SEM images on top corresponds to low (left) and hight (right) temperature plasma treatment. The scatter plots on the bottom corresponds to the SEM images on top and show the evolution of nanowire length as a function of the diameter. The violin plots show the statistical distribution. The In Flux is $3.1x10^{-8}$ Torr and As Flux is $2.4x10^{-5}$ Torr . Growth temperature is 410 °C. Scale bars is 500 nm.*

4.5.1.3 Influence of the amount of Hydrogen

In order to asses the plasma treatment influence, five different samples were grown using different Hydrogen fluxes: 0.5, 1, 2, 3 and 5 sccm (plasma ignited at 250W and 200 °C for1 hour) and keeping the growth conditions identical. Prior to nanowire growth, the five samples were ramped up and annealed at 650°C (20 minutes) under an arsenic flux of $2x10^{-5}$ Torr. The temperature was then lowered to 410 °C under the same As environment, and the growth was initiated changing the arsenic flux to $1.2x10^{-5}$ Torr and opening the indium shutter (flux of $3.1x10^{-8}$ Torr) for 1 hour. The figure 4.6 presents the statistics obtained for these five growth: the scatter plot represents length and diameter of each nanowire, while the violin plot shows the statistical distribution. The large distribution in length and diameter originates from a nanowire nucleation that can occurs from t=0 to t=60 minutes, but the slope of each scatter plot, which corresponds to the aspect ratio, remains almost constant. No clear influence of the hydrogen amount on nanowire growth can be measured from this study, and thus the hydrogen flux is fixed to 1 sccm in the following (better stability for the plasma cell).

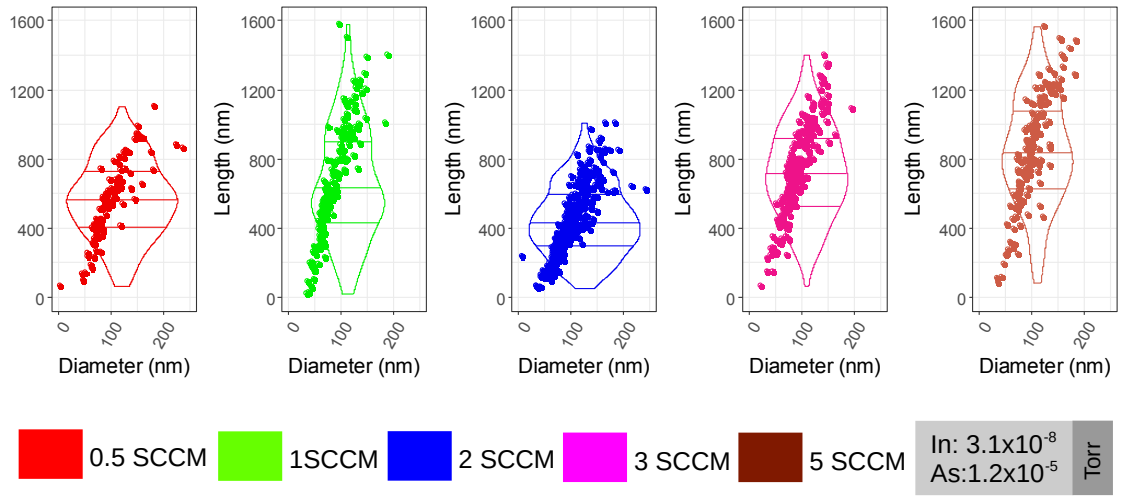


Figure 4.6 – *Scatter and violin plots representing the influence of the hydrogen amount. The scatter plots show the evolution of nanowire length as a function of the diameter and the violin plots show the statistical distribution for different hydrogen fluxes: 0.5, 1, 2, 3, 5 sccm respectively. The In flux is $3.1x10^{-8}$ Torr and As flux is $1.2x10^{-5}$ Torr. The growth temperature is 410 °C.*

4.5.1.4 Influence of the Arsenic Treatment Temperature

As reported in section 4.4, it is widely accepted that a high temperature annealing under arsenic is necessary for creating a Si(111)B surface by breaking the Si-H bounds and forming a final Si-As layer. This high temperature annealing seems to be dependent of the growth system from 950 °C for Tomioka et al.[206] to 630 °C for Wang et al.[239]. The reported temperatures are always above or at least 500°C[203,206,207,225–233,239], which is detrimental for BEOL processes. It is thus mandatory to address this bottleneck to allow full CMOS compatibility. If verticality and yield of self-catalyzed nanowires integrated on silicon have been widely studied, the thermal budget remains a big unaddressed issue. Indeed, if InAs or InSb[7,236,240–242] nanowire growth occurs at temperatures lower than 450°C, the substrate preparation, prior to growth, always crosses this limit.

In order to address this issue, three sample have been grown using annealing temperatures of respectively 650°C, 500°C and 450°C. Apart from this annealing temperature under arsenic, the hydrogen preparation and growth conditions remained identical from sample to sample (1 sccm of H_2 plasma ignited at 250W at 200 °C for 1 hour). SEM images presented in figure 4.7, show that InAs nanowires are always vertical, but that their density, length and diameter are influenced. This first result proves that a BEOL compatibility is achievable but the growth conditions need to be optimized in order to get high densities and good aspect ratios. This is what will be developed and discussed in the following sections.

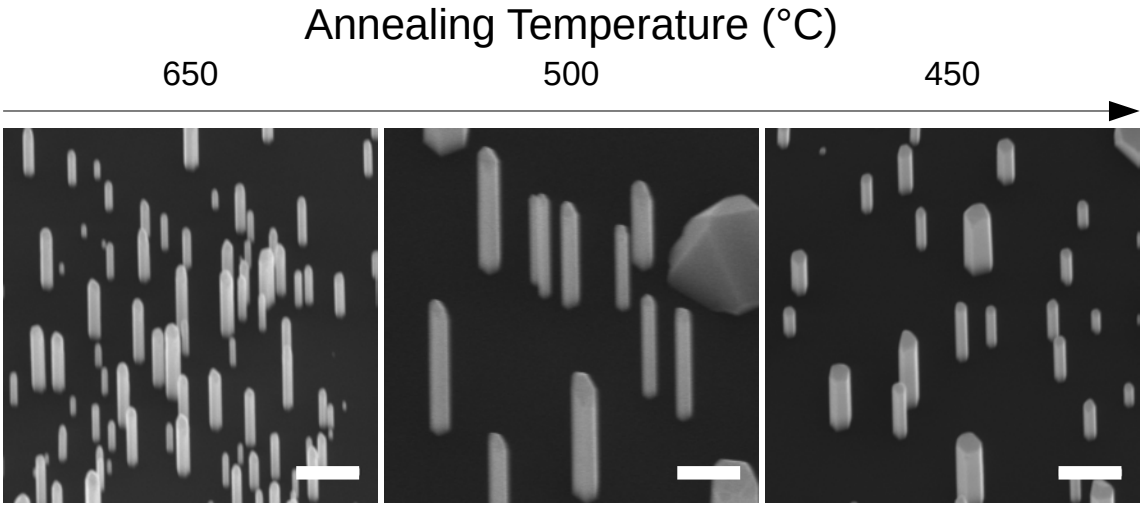


Figure 4.7 – *Influence of the in-situ annealing under arsenic on nanowire growth. The SEM images present as-grown wafers for different annealing temperatures: from 650°C (left) to 450°C (right). The In flux is 3.1x10^{-8} Torr and As flux is 1.2x10^{-5} Torr. The growth temperature is 410 °C. Scale bars are 500 nm.*

4.5.2 Full CMOS Compatible InAs Nanowires

In this section, we investigate the influence of the substrate preparation environment on the growth of InAs nanowires by MBE and propose a fully CMOS compatible process for the integration of III-V nanowires on silicon without passing the 450°C limit. This section is organized as follows. First the experimental process is presented. Next, the SEM analysis of samples having the same growth conditions but different surface preparation treatments is discussed. Then the nature of the hydrogen (gas/plasma) is probed. A detailed statistical analysis taking into account at least 150 nanowires from each of the sample follows next. After these, the TEM analysis reveals the nanowires growth mode depending on the surface preparations. This section ends with AFM measurements to probe the influence of the surface preparation on its roughness.

4.5.2.1 The Experimental Description

Self-catalyzed InAs nanowires are grown on commercially available 2 inch NID Si(111) wafers from Siltronix in a solid-source MBE system (RIBER-MBE412). Once the native oxide is removed with the help of hydrofluoric acid (HF 5%), substrates are immediately loaded into the MBE chamber. The degassing of these wafers is carried out at 200°C for 1 hour under an Hydrogen flux: we use either a 1 sccm flux of Hydrogen gas or a 1 sccm flux of Hydrogen plasma (RF source and Power=250W). Next, the substrates are loaded into the growth chamber where they are directly heated up to the growth temperature (410°C) under an arsenic flux of 2.10^7 Torr for 1 hour. Finally, the nanowire growth is initiated by opening the In shutter for 1 hour. The different fluxes we used during this study are 0.8 $x10^{-8}$, 1.5 $x10^{-8}$ and 3.1 $x10^{-8}$Torr for indium and 1.2 $x10^{-5}$, 1.8 $x10^{-5}$ and 2.4 $x10^{-5}$ Torr for arsenic. Note that an In flux of 3.1 $x10^{-8}$ Torr corresponds to growth rate of 0.02 monolayer/sec on GaAs and an As flux of 2.4 $x10^{-5}$ Torr corresponds to a growth rate of 1 monolayer/sec on GaAs. After growth, the nanowires are cooled down to 200°C using the same arsenic flux. The nanowires were characterized by Scanning Electron Microscopy (SEM, FEI Aztec-600i) and Transmission Electron Microscopy (TEM), using a JEOL 2100F with field emission gun for high resolution analysis (HRTEM) and a JEOL Cold FEG probe-corrected ARM200F for STEM/HAADF and STEM/EDX analysis. Strain maps were calculated using the open source Strain++ program based on the Geometric Phase Analysis (GPA) algorithm by Hytch et al.[243].

4.5.2.2 The SEM Analysis: influence of the surface preparation on nanowire growth

Figure 4.8 presents SEM images of samples having the same growth conditions (i.e. same arsenic flux, indium flux and growth temperature) but different surface preparations (HF etching, Annealing at high or growth temperature, H_2 surface preparation during wafer degassing). Interestingly, and as reported before[206], the chemical etching of the native oxide with HF is mandatory to achieve growth of vertical nanowires [figure 4.8(c,d,e,f)]; but not the high temperature annealing under arsenic flux [figure 4.8(c,e)]. The opposition between these observations and the literature about MOVPE InAs nanowire growth should originate from the growth environment differences between MBE and MOVPE (H_2 and pressure), leading to a faster re-growth of the native oxide in a MOVPE

reactor[203,206]. Moreover, samples with H_2 preparation [figure 4.8(e,f)] have always a better aspect ratio (thinner wires) compared to other samples. This originates from different surface terminations after the H_2 preparation leading to different diffusion lengths of elements III on the substrate surface. Consequently, crossing the BEOL temperature limit to grow fully vertical self-catalyzed InAs nanowires on silicon is not needed [figure 4.8(e)] and using a pre-growth hydrogen treatment leads to thinner wires. The H_2 environment during substrate degassing is expected to increase the indium diffusion length by filling dangling bonds. This could explain the differences observed between MBE and MOVPE growth of InAs nanowires[203,206,225–233,236–238] since H_2, which is the carrier gas in MOVPE reactors, is lacking during MBE growth.

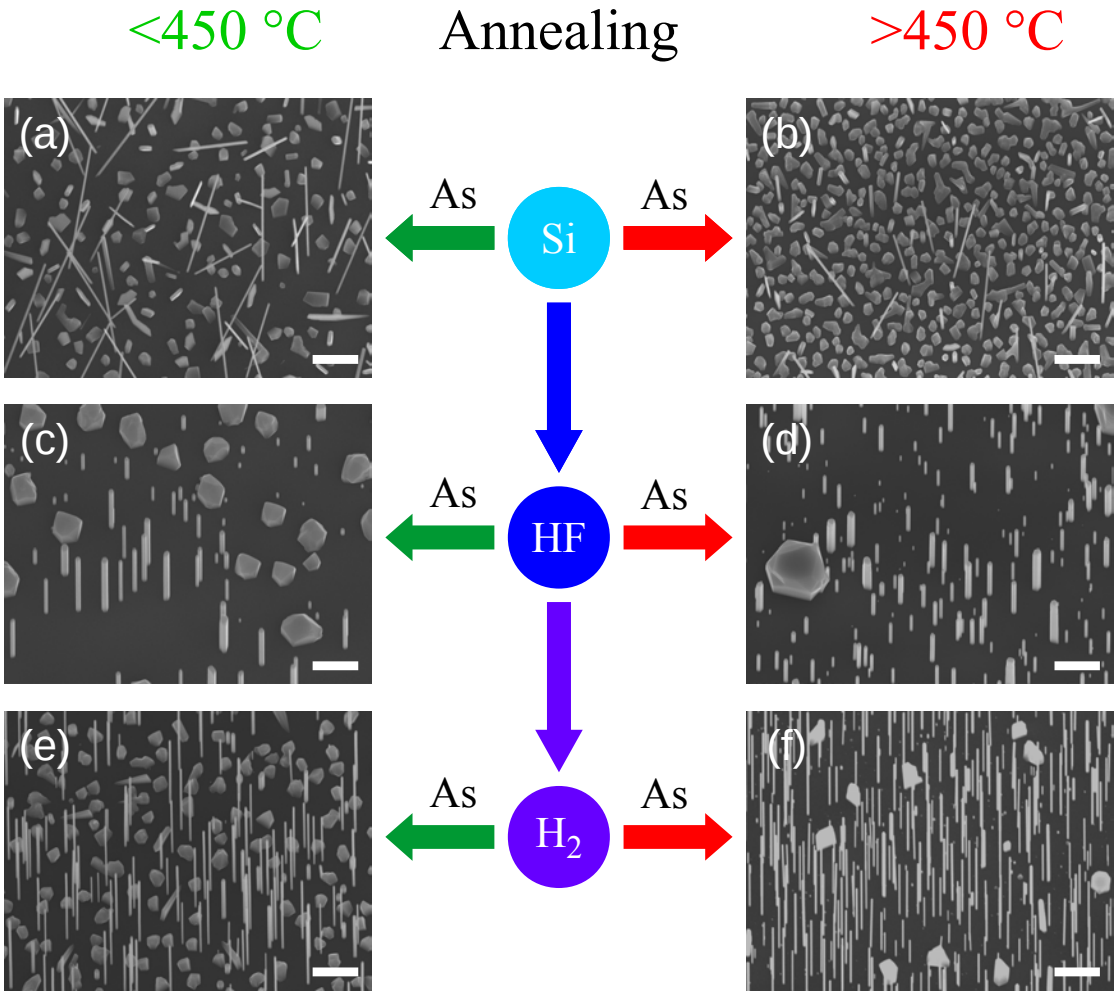


Figure 4.8 – *Surface preparations and nanowire growths. (a) to (f) SEM images of InAs nanowires grown on silicon (111) wafers using the same growth conditions but different surface preparations. The processes are divided in two: (a), (c) and (e) are compatible with the BEOL limitations with an in-situ annealing at growth temperature whereas (b), (d) and (f) are annealed at higher temperature. For (a) and (b), the native oxide is present when samples are loaded into the growth chamber. For (c) and (d), the native oxide is removed using an HF5% solution for 1 minute prior to the loading into the MBE reactor. For (e) and (f), a flux of hydrogen is used during the sample degassing (after the native oxide removal). The scale bars correspond to 500 nm.*

Moreover, it is also possible to initiate or not the plasma, during the hydrogen preparation and thus having either a H_2 gas or a H_2 plasma treatment. This is reported in figure 4.9, where SEM images of eight samples having different surface preparations: plasma (in red box) and gas (in green box) are reported for four set of growth parameters. The indium flux increases from bottom to top, while the arsenic flux increases from left to right. First, we can notice that all wires are vertical irrespective of the surface treatment confirming complete removal of native oxide. Moreover, we can note that nanowires on gas treated surfaces are thinner and longer than their counterpart on plasma treated surfaces. The nanowire density is highly promising on the gas treated surface when both In and As fluxes are high [figure 4.9(c)]. In contrast , the formation of big islands is clearly visible on the plasma treated surface with same growth parameters [figure 4.9(d)]. This further confirm the major influence of the surface preparation on nanowire growth. On the contrary, when a low indium flux ($1.5x10^{-8}$ Torr) is used, the two surfaces seem to be equivalent in terms of nanowire morphology and density [figure 4.9(e, f, g and h)].

These differences could be explained by a different chemical potential on both surface. Indeed, in a self-catalyzed growth process, the nanowire morphology and density depend strongly on the diffusion length of group III element on the surface. If the quantity of indium is low, the system kinetics is reduced, which allows indium atoms to travel longer distances on the surface. On the contrary, when both indium and arsenic are increased, the influence of the chemical potential are dramatically increased. This clearly indicates that both processes result in different surface terminations.

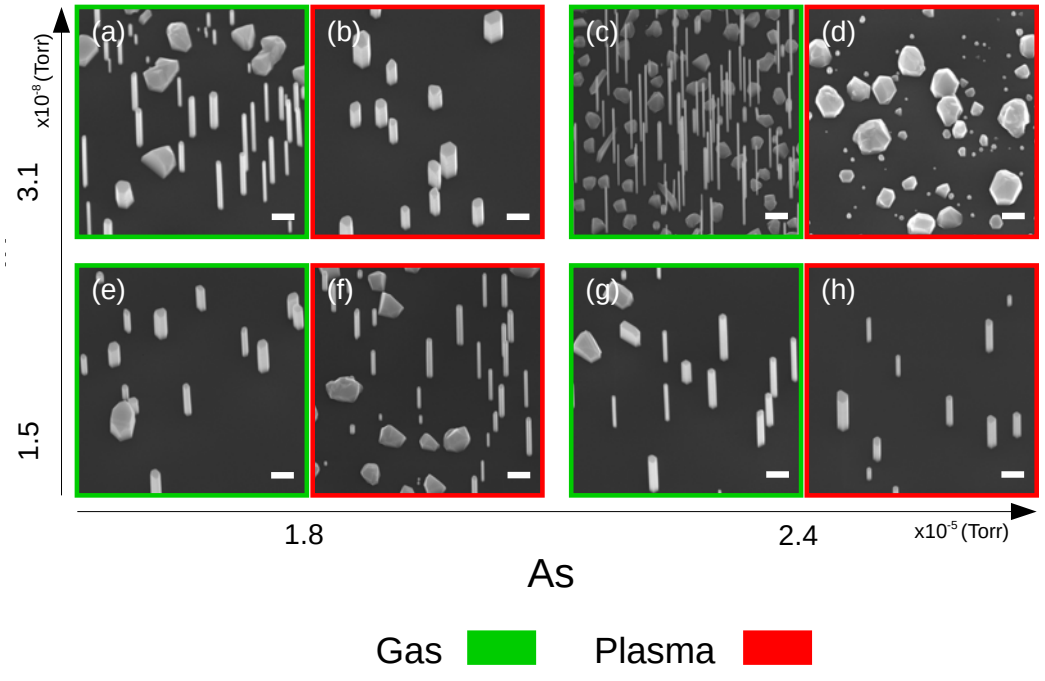


Figure 4.9 – *SEM images of InAs nanowires grown on Si(111) wafers using four set of growth conditions and different surface preparations. The H_2 gas treated surfaces are framed by green boxes (a,c,e,g), whereas it is red(b,d,f,h) in the case of a H_2 plasma preparation. Scale bars correspond to 500 nm.*

4.5.2.3 The Statistical Analysis of the Nanowires Morphology

In order to characterize the influence of the hydrogen preparation on the InAs NW growth, a complete growth study was performed using the figure 4.8(e) surface preparation as a starting point. Here, all samples are degas at 200°C for 1 hour under an hydrogen gas flux, and an in-situ annealing under arsenic for 1 hour is performed at growth temperature (~410°C). From each sample, more than 150 nanowires were characterized using the method described in chapter 2, section 2.4. Creating families of homogeneous diameters (the x axis of each graph in figure 4.10), it is possible to perform statistics and plot the length and the percentage of each family for different indium and arsenic fluxes as reported in figure 4.10. As already mentioned in the literature[244], the nanowires diameter decreases when the arsenic flux is increased (see the probability part of figure 4.10), whatever the indium flux is. This is consistent with other MBE studies about InAs nanowires growth[238] and a self-catalyzed growth mechanism (Vapor Solid growth mechanism). Interestingly, when the indium and arsenic fluxes are both increased simultaneously (3.1 x10^{-8} Tor for In and 2.4 x10^{-5} Torr for As), long and thin nanowires can be obtained. This "abnormal" behavior can be explained by a change of in the growth mechanism from Vapor Solid (VS) to Vapor Liquid Solid (VLS) as already reported for InP nanowires[245]. Consequently, obtaining "clean" substrate surfaces thanks to the hydrogen preparation and optimizing the growth conditions, makes it possible to maximize the aspect ratio of VLS InAs nanowires on silicon.

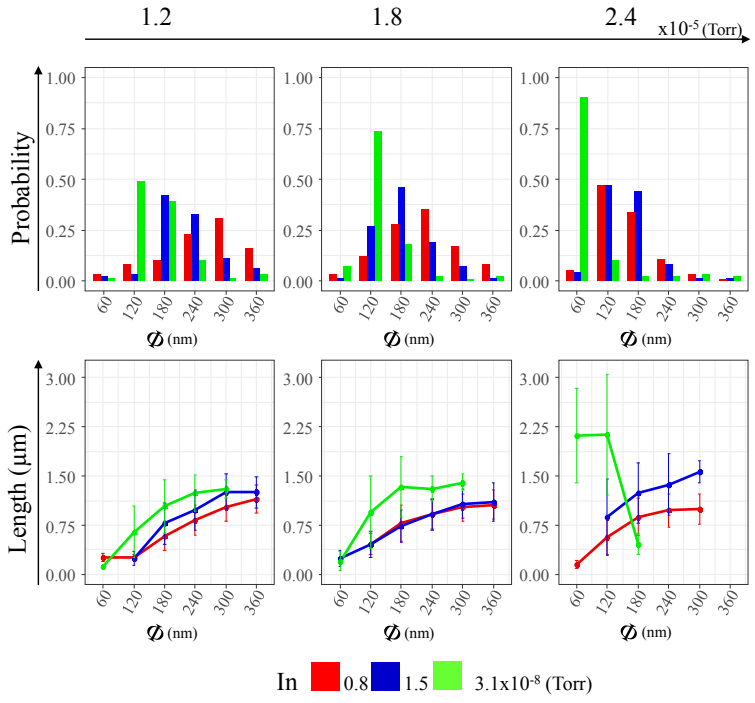


Figure 4.10 – *Statistic plots for the H_2-gas treated surfaces corresponding to the figure (1e) process. Nanowires are grouped in families of different diameters (See chapter 2 section 2.4). The three colors (red, blue, green) correspond to different indium fluxes. On top, the proportion of each family is reported as a function of the arsenic flux. On bottom, the mean length of each family is reported as a function of the arsenic flux. These statistic graphs allow to evaluate the influence of the indium and arsenic fluxes on the diameter and the length of the InAs nanowires.*

Next, the nature of the surface preparation (either gas or plasma) was assessed thanks to a full quantitative analysis of nanowire growth. In that purpose, all the growth conditions investigated in for figure 4.10 have been repeated in the case of the H_2-plasma preparation. Using the procedure presented in chapter 2 section 2.4, more than 150 nanowires were measured for each sample, and nanowire diameter categories were created for both plasma (in red) and gas (in green) treated surfaces.

Figure 4.11 presents the occurrence probability of each family as a function of the indium and the arsenic fluxes. Whatever the surface treatment is, increasing indium or arsenic results in reducing the nanowire diameter as reported in literature[244]. This can be explained by near equilibrium conditions, where kinetics drives nanowire growth. Moreover, in the case of a H_2-gas preparation and for the highest indium and arsenic fluxes ($3.1x10^{-8}$ and $2.4x10^{-5}$), almost all nanowires have a diameter of 60nm, contrary to a H_2 plasma treatment. This unconventional behavior, as previously reported in figure 2.4(c), is the signature of a different growth process (VLS) compared to other samples (VS).

Similarly, we now report nanowire length for each of these families (figure 4.12) as a function of the diameter for each substrate preparation (i.e. Gas in green and Plasma in red). As in figure 4.11, the arsenic flux increases from left to right and the indium one from bottom to the top. First, a general trend can be observed: there is an global increase of the nanowire length with its diameter; except for the VLS sample (high indium and arsenic fluxes and H_2 gas preparation). This can be explained by nanowires nucleating at different time between 0 and 60 minutes. In VS growth, since the group III droplet is consumed at an early stage, the sidewall growth becomes prominent and diameter increases a lot. In contrast, the VLS growth mode of the H_2 gas sample, having the highest indium and arsenic fluxes, lead to very thin (<60nm) (figure 4.11) and long (3 µm) wires (figure 4.12). When the liquid droplet is preserved, the high difference of chemical potential between the catalyst and the substrate surface allows an efficient collection of material and fast vertical growth. This further suggests, that the total amount of material (In and As fluxes) is more important than just the V/III ratio, and that surface diffusion and chemical potentials are kinetically driving this.

Finally, another way of presenting these results proposed in figure 4.10, 4.11 and 4.12 is to construct a scatter plot taking all the nanowires that were measured for the analysis. The figure 4.13 presents a direct comparison of the length and diameter of wires grown on H_2-gas and H_2-plasma surfaces. In these scatter plots, we clearly see that a difference arises when increasing both arsenic and indium fluxes. Although the H_2-gas and H_2-plasma preparations are not expected to give dramatically different surfaces, major changes are observed. While H_2-gas treated surfaces favor long and thin wires when indium and arsenic fluxes are increased, the opposite is observed for H_2-plasma treated surfaces. This could be explained by a filling of the dangling bonds and a smoother surface for the H_2-gas preparation in opposition with the H_2-plasma one. Indeed, the element III diffusion length appears to increase for a H_2-gas prepared surface leading to a change of the growth mechanism from VS to VLS.

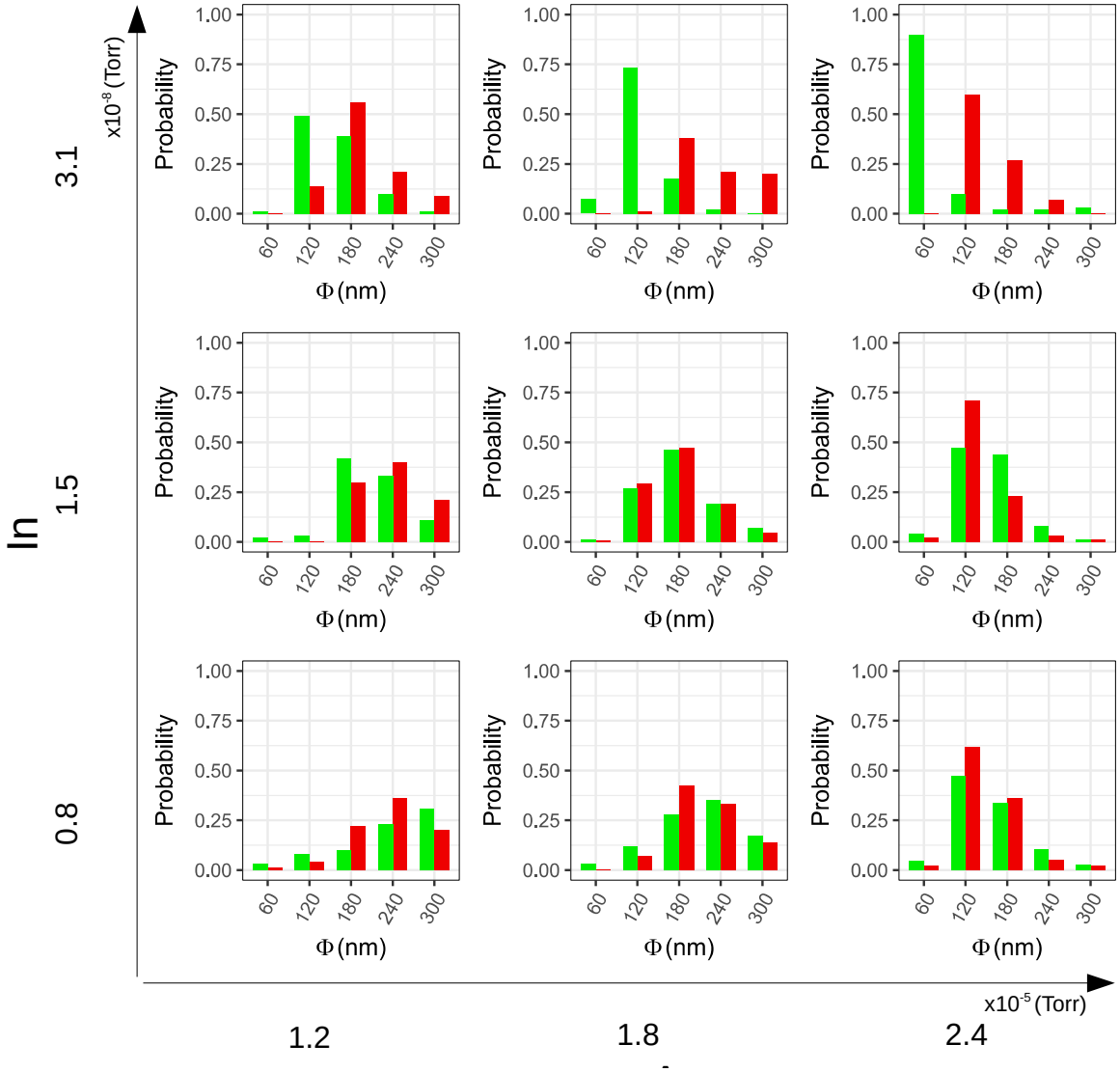


Figure 4.11 – *Comparisons between the H_2-gas (in green) and H_2-plasma (in red) surface preparations. Each of the 9 scatter plots correspond to a specific growth condition associated with the arsenic and indium fluxes reported on bottom and on left. For each plot, the x-axis corresponds to the diameter and the y-axis to the probability of occurrence. Each bar represents the occurrence probability of a diameter-based nanowire family for both H_2 gas (in red) or H_2plasma (in green) surface preparation [figure 4.8(e)]. Red and green bars are almost superimposable for low indium and arsenic fluxes, but are well separated for high indium and arsenic fluxes.*

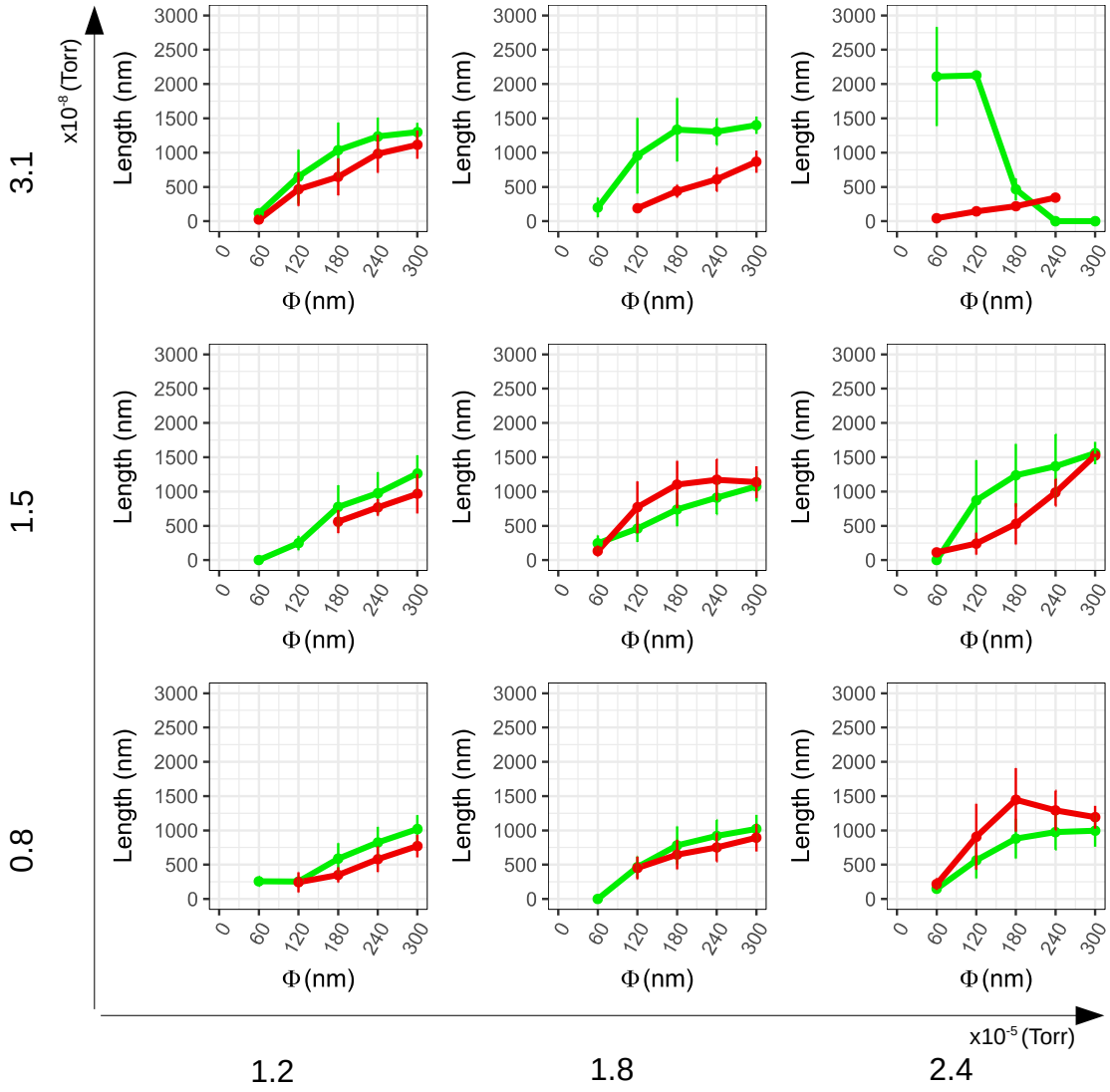


Figure 4.12 – *Comparisons between the H_2-gas (in green) and H_2-plasma (in red) surface preparations. Each of the 9 scatter plots correspond to a specific growth condition associated with the arsenic and indium fluxes reported on bottom and on left. For each plot, the x-axis corresponds to the diameter and the y-axis to the length. Each point represents the length of a diameter-based nanowire family for both H_2 gas (in red) or H_2plasma (in green) surface preparations [figure 4.8(e)]. Red and green lines are almost superimposable for low indium and arsenic fluxes, but are well separated for high indium and arsenic fluxes.*

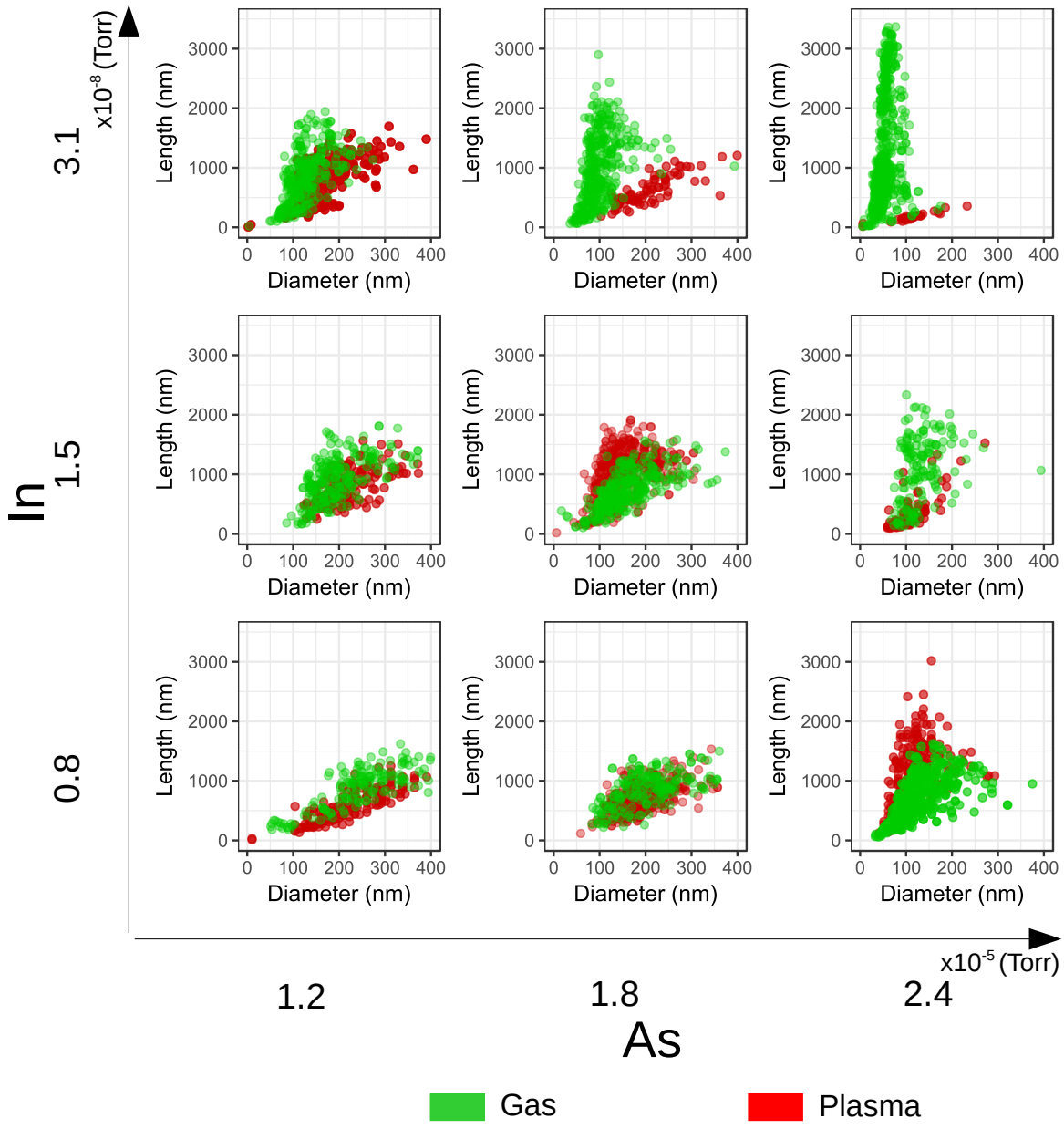


Figure 4.13 – *Comparisons between the H_2-gas (in green) and H_2-plasma (in red) surface preparations. Each of the 9 scatter plots correspond to one specific growth condition associated with the arsenic and indium fluxes reported on top and on right. For each plot, the x-axis corresponds to the diameter and the y-axis to length of the nanowires. Each point represent an unique nanowire measured either for the H_2-gas (in red) or the H_2plasma (in green) surface preparation (figure 1(e)). Red and green points are almost superimposable for low indium and arsenic fluxes but are well separated for high indium and arsenic fluxes.*

4.5.2.4 The TEM Analysis

The structural investigation of the InAs nanowires grown in figure 4.8(e), was performed in a TEM. The crystalline structure was first analyzed by HRTEM on nanowires that were mechanically transferred on a carbon holey grid. As generally observed[7], the measured InAs nanowires (4.14) grow along the <111> direction and are composed of a mixture of wurzite (WZ) and zinc-blende (ZB) segments. Interestingly, the bottom region exhibits a majority of ZB segments separated by several twin planes whereas the top of the nanowires contains more WZ regions.

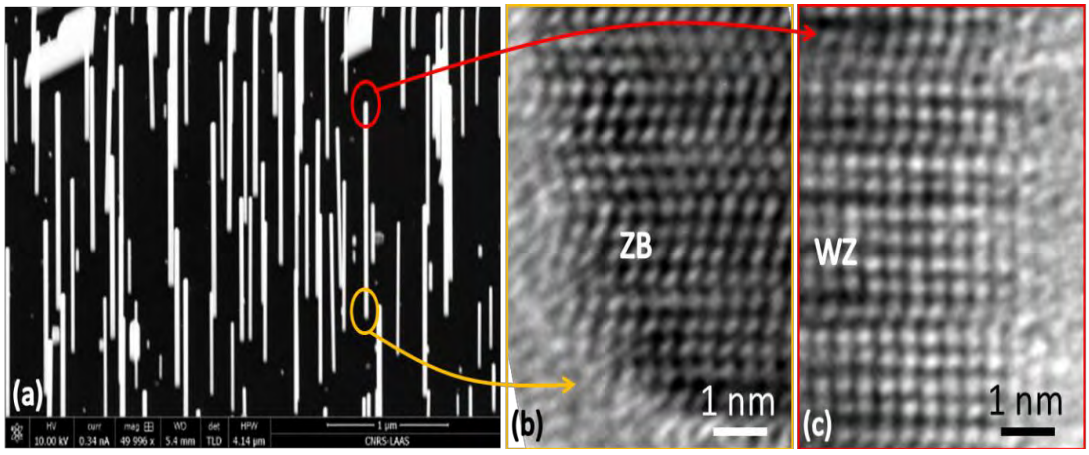


Figure 4.14 – *(a) SEM image of InAs NWs grown on a Si(111) substrate (figure 4.8 e). (b) and (c) HRTEM micrographs taken respectively from the bottom and top region of a InAs NW. InAs NWs are found to grow along the <111> direction and are composed of a mixture of wurzite (WZ) and zinc-blende (ZB) segments. Interestingly, the bottom region (b) exhibits a majority of ZB segments separated by several twin planes whereas the top of the NWs (c) contains more WZ regions; The difference in contrast between the atomic layers contained in the InAs planes clearly indicates that the InAs NWs exhibit a B-type surface (i.e. As-terminated).*

Figure 4.15 presents structural investigation of the nanowire tip carried out by HR-TEM once the wires were mechanically transferred onto the holey-carbon grid. Interestingly, except for the sample corresponding to figure 4.9 (c), the nanowire top is completely flat [4.15 (c) & (d)], indicating the absence of the In droplet. In contrast, the round curvature at the end of the nanowires in figure [4.15 (a) & (b)], confirms probable VLS growth mode for this sample. The presence of a droplet during the growth should improve the nanowire aspect ratio in that case. This further highlights the change of growth mode from VS to VLS by varying the surface treatments depending upon the nature of H_2 (gas or plasma). Moreover, the VLS growth mode for the nanowires with high In and As flux further suggests that diffusion length of In should be higher on gas treated surfaces, allowing to collect more material on these surfaces.

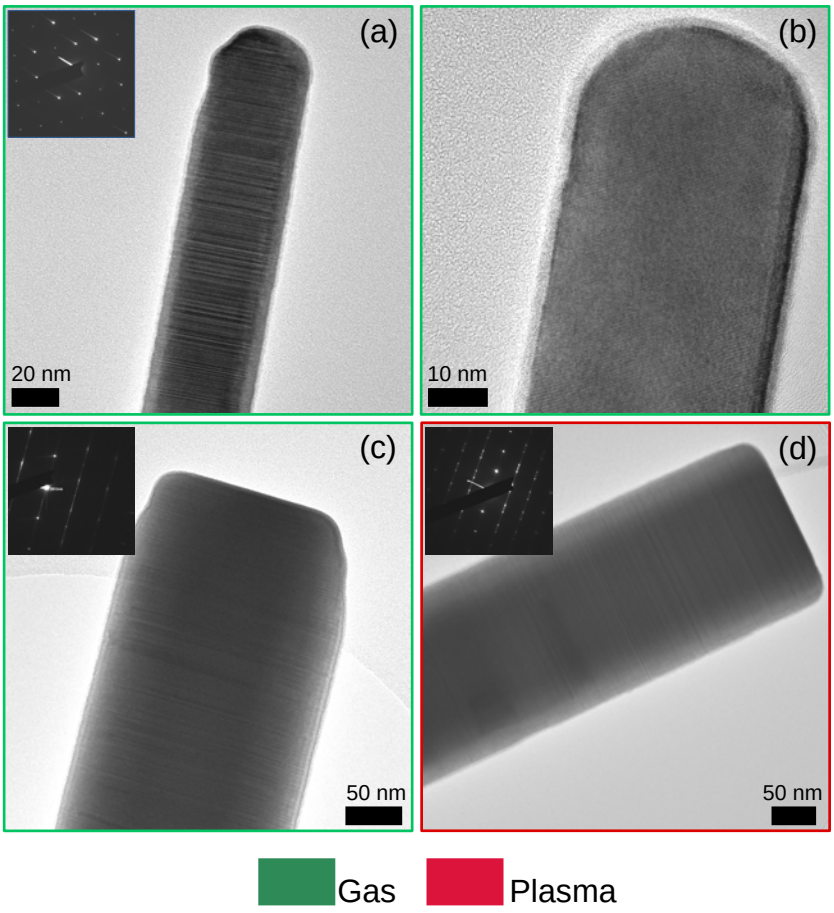


Figure 4.15 – *HRTEM micrographs taken at the top regions of InAs nanowires. (a) & (b) correspond to InAs NWs from 4.9 (c), (c) & (d) respectively correspond to 4.9. [(e) & (f)]. (a), (c) and (d) are viewed along [110] while (b) is viewed along [112]. The growth direction is <111> in all the cases.*

Subsequently, cross-sectional TEM measurements with InAs nanowires still attached to the Si substrate were performed thanks to a Focused Ion Beam (FIB) preparation. This allows to take STEM/HAADF images at the interface between InAs nanowires and the Si substrate, and thus to assess the interface quality. To this purpose, nanowires are coated with amorphous carbon prior to FIB preparation, but, as shown in figure 4.16(a), the non-uniformity in the carbon deposition on each side of the nanowires (cf. white arrows) may result in strain-induced bending (cf nanowire on the left-hand side in figure 4.16(a). In the case of long nanowires (~2 µm), the induced strain can even exceed the plastic deformation threshold (~5 GPa for traction fracture in InAs nanowires[246,247]) and dislocations are therefore formed close to the InAs/Si interface (C.1).

The interface analysis was therefore performed on small nanowires (length <100nm) where bending effects are negligible [figure 4.16(a)]. A typical image of the InAs/Si interface region, obtained by STEM/HAADF is shown in figure C.1 (Appendix C). The InAs and Si layers are perfectly aligned and are separated by a weak contrast band corresponding to the native SiO_2 layer which covers the Si surface around the nanowire (as schematically shown in figure D.1). Such layer weak-

ens the image contrast but does not stop the atomic planes to be visible throughout the interface in STEM/HAADF images [figure 4.16(b,c,d)], clearly indicating that InAs growth occurs epitaxially on the Si substrate. In addition, along the direction parallel to the interface, about 9 InAs (111) planes are observed for every 10 corresponding Si (111) planes [figure 4.16(b)], in agreement with the difference in the lattice constant of ZB InAs (6.058 Å) with respect to Si (a[Si]/a[InAs] = 0.897). The InAs nanowires can therefore be considered as fully relaxed and misfit dislocations are expected to form, as enlightened by the Burgers circuit in figure 4.16(c) (showing an isolated misfit dislocation) or by the Geometrical Phase Analysis (GPA) method applied to a lower magnification image [figure 4.16(d and e). In this case, five dislocations are observed within a distance of ~11 nm along the interface, again in agreement with a complete relaxation of the InAs lattice. Consequently, the proposed surface preparation [figure4.8(e)] leads to the fully relaxed epitaxial growth of InAs nanowires on silicon respecting a 410°C thermal budget.

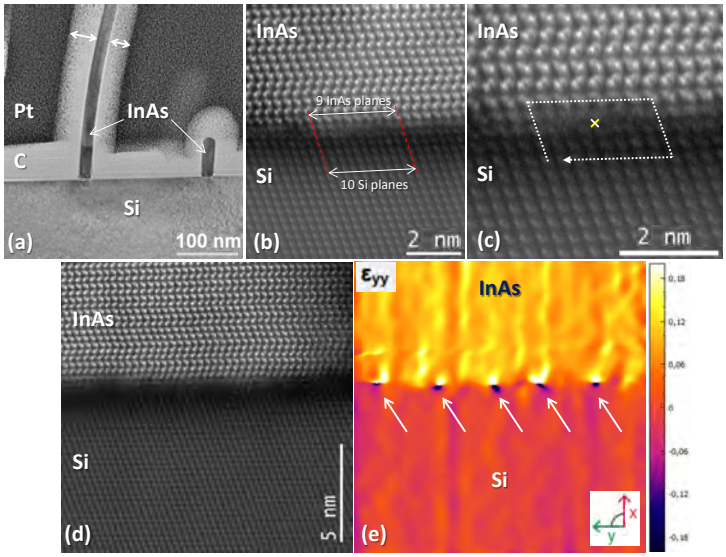


Figure 4.16 – *(a) Cross-section TEM image of InAs nanowires still attached to the Si(111) substrate. Non-uniformity in the carbon deposition on each side of the nanowires (cf. white arrows) may result in stress-induced bending of long nanowires (cf. nanowire on the left of the image). (b), (c), (d) STEM/HAADF images taken at the interface between an InAs nanowire and the Si substrate indicating that the InAs growth occurs epitaxially on the Si substrate. The weak contrast band located at the InAs/Si interface corresponds to the native SiO_2 layer covering the Si surface around the nanowire (cf. Appendix D). (b) Along the direction parallel to the interface, about 9 InAs (111) planes are observed for every 10 corresponding Si (111) planes, in agreement with the ratio between the lattice constants of InAs and Si (a[Si]/a[InAs] = 0.897). The InAs nanowires can therefore be considered as fully relaxed. (c) A Burgers circuit drawn at the InAs/Si interface allows to identify the position of an isolated misfit dislocation. (d) STEM/HAADF image of the InAs/Si interface region and (e) corresponding strain mapping (ε_{yy}) in the direction parallel to the interface obtained by GPA. Five dislocations are visible within a distance of ~11 nm along the interface, in agreement with a complete relaxation of the InAs lattice.*

4.5.2.5 AFM Measurements of the Surface Roughness

In order to probe the influence of the hydrogen preparation, three samples were inspected with an Atomic Force Microscope (AFM) (Figure 4.17 and Table 4.4). Once the native oxide is removed with an HF 5%, the samples are loaded directly into the MBE system and are degassed at 200 °C for one hour. Three degassing environment were considered: first the normal degassing at 200 °C, second the degassing at 200 °C for 1 hour under H_2 gas (1 sccm) and third the degassing under 1 sccm of H_2 plasma (RF Sourced -250 watt). The AFM measurements were carried out immediately once the samples are unloaded from the MBE system. The measurements, from figure 4.17 and table 4.4, do not highlight any substantial difference regarding the sample roughness as the Root Mean Square Deviation Rq varies only by a few 0.01 nm. From these evidences, we conclude that the H_2 treatment is not affecting significantly the surface roughness.

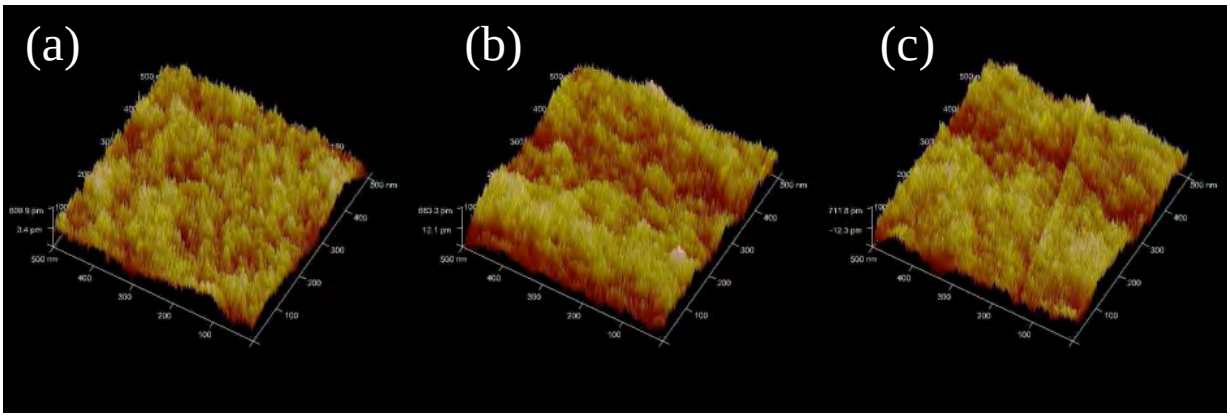


Figure 4.17 – *AFM measurements of the Si(111) roughness (a) reference sample degassed at 200 °C after oxide removal, (b) degassing under H_2 plasma at 200 °C and (c) degassing under H_2 gas at 200 °C. The degassing time is 1 hour. All acquisition scans are performed a squared surface of 500x500 nm^2.*

Sample	RQ (Plane)	RQ (Flat)
200 °C degassing	0.19 nm	0.18 nm
200 °C degassing under H_2 gas	0.25 nm	0.20 nm
200 °C degassing under H_2 Plasma	0.22 nm	0.21 nm

Table 4.4 – *Surface roughness from the AFM measurements. RQ represents Root Mean Square (RMS) measurement on roughness while plane and flat stand respectively for hard and soft image processing algorithm that software implements during the image acquisition.*

4.5.3 The DFT Analysis

In order to understand the role of Hydrogen and Arsenic on the Si(111) surface during nanowire nucleation, we performed Density Functional Theory (DFT) calculations, in collaboration with a Master student: Nicolo Sartori.

4.5.3.1 Details on DFT Calculations

The periodic calculations were performed using the DFT method based on the GGA approximation employing the PBE exchange-correlation functional as implemented in the plane-waves program VASP[248–250] . The projector-augmented wave (PAW) potentials were applied for the core electron representation[251,252] . A converged value of Ecut = 500 eV was used for the cut-off energy of the plane wave. The Γ point is used to sample the Brillouin zone. The integration in reciprocal space was performed with a Monkhorst-Pack grid[253].

The Si(111) surface is modeled as a repeated $Si_{192}H_{16}$ slab. The silicon substrate is formed with twelve layers of sixteen silicon atoms as a (4x4) simulation supercell. Hydrogen atoms are placed to passivate the dangling bonds of the silicon atoms below the slab. A vacuum zone of 20 Å in the z direction was used to create a surface effect. The final cell dimensions are 15.46 x 15.46 x 38.93 $Å^3$ with a surface area of 239.01 $Å^2$. The periodic slab is repeated in the three directions. These simulation cell parameters have been checked to avoid any interaction with other periodic cells. The six bottom layers of the slab and hydrogen atoms are kept fixed to simulate the bulk, all other atoms are free to relax. Nudged Elastic Band method is used to calculate activation barriers[254–257].

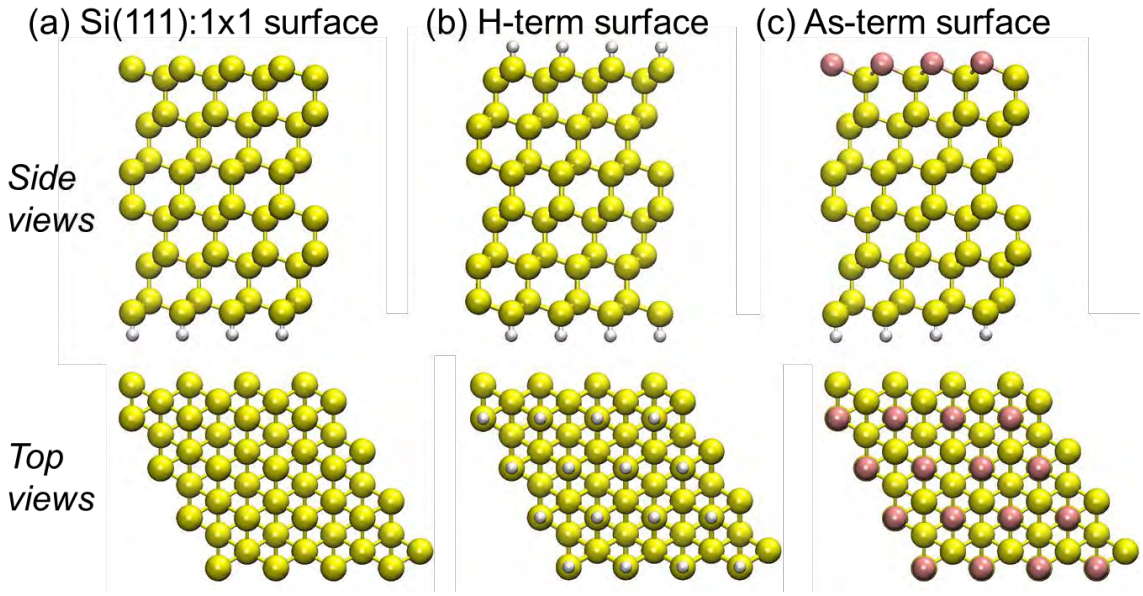


Figure 4.18 – *Side and top views of (a) Si(111):1x1 slab, (b) H-terminated Si(111):1x1 surface and (c) As-terminated Si(111):1x1 surface. Yellow, white and pink spheres are respectively Si, H and As atoms.*

4.5.3.2 Considered Surfaces for DFT Calculations

From Si(111) surface [figure 4.18(a)], two surface preparations are used [figure 4.18(b)] and Side and top views of (a) Si(111):1x1 slab, (b) H-terminated Si(111):1x1 surface and (c) As-terminated Si(111):1x1 surface. Yellow, white and pink spheres are respectively Si, H and As atoms). The H-terminated Si(111):1x1 surface is created by adsorbing a full layer of H atoms on top of the topmost of the silicon substrate and the As-terminated Si(111):1x1 is created by substituting the topmost silicon layer of the silicon substrate by an As layer. In addition to the two modeled surface treatments already described in the manuscript, an arsenic treatment where As atoms adsorbed to fill the Si dangling bonds of the Si(111) surface, was also considered. However, such a configuration generates a heavy reconstruction of the layer itself because it has to reduce its own dangling bonds and results in non-vertical nanowires, consequently this option was discarded. Otherwise, creating indium droplets on the surface prior to nanowire growth does not improve nanowire nucleation, so the corresponding surface has not been considered.

4.5.3.3 Adsorption reaction and energy

Adsorptions of one In or As atom is thus performed considering the topology of such prepared surfaces. The isolated In or As atoms were relaxed in the same simulation cell as the Si(111) slab to obtain the reference value of the atomic species. Initially, ad-atoms are placed 2 Å far from the topmost layer and free to relax. The adsorption sites were identified by screening the topology of the Si(111) surfaces. When looking at the Si(111) surface from the top, i.e. along the <111> direction, the surface highlights different adsorption sites, that can be distinguished by considering the layer stacking and surface topology [See figure 4.19(a)].

In this chapter the adsorption energies ΔE_{ads} are calculated using the following formula:

$$\Delta E_{ADS} = E_{AtomOnSiSlab} - E_{SiSlab} - E_{IsolatedAtom} \tag{4.8}$$

where E_{SiSlab} is the total energy of the relaxed H-terminated Si(111):1x1 and As-terminated Si(111):1x1 surfaces. $E_{AtomOnSiSlab}$ is the total energy of the system with an In or As atom adsorbed on the Si(111) surface obtained considering the HF or As treatment, $E_{IsolatedAtom}$ is the total energy of the isolated atom (either In or As). Conventionally, negative values indicate exothermic adsorption.

4.5.3.4 The DFT Discussion

In order to understand the role of Hydrogen and Arsenic on the Si(111) surface during nanowires nucleation, we performed Density Functional Theory (DFT) calculations as reported in figure 4.19. In these simulations, we model the Si(111) surface using a (4x4) simulation cell (Details of calculations are given in section 4.5.3.1). Two different surface terminations depending on the surface treatments are considered (figure 4.18). From literature, we know that HF etching and degassing leave the surface mainly covered with hydrogen[258], so an H-terminated Si(111):1x1 surface is considered, where H atoms fill the dangling bonds of the topmost silicon layer [figure 4.18(b)]. Considering the

in-situ arsenic preparation, an As layer substituting to the topmost layer of Si substrate was used, commonly referred as the As-terminated Si(111):1x1 reconstruction [figure 4.18(c)]. Such surface has already been studied in detail experimentally[259,260] revealing that an As-terminated Si(111):1x1 prevents the Si 7x7 reconstruction. Ab-initio calculations about the precise As position with respect to the silicon matrix have already been performed[261,262] fitting with our model (Si-As bond length of 2.46 Å). It is worth noting that this structure is so stable that it is often considered as an effective passivation of the silicon surface. Other surfaces were investigated and appeared not to be relevant for this study (comments given in figure 4.19).

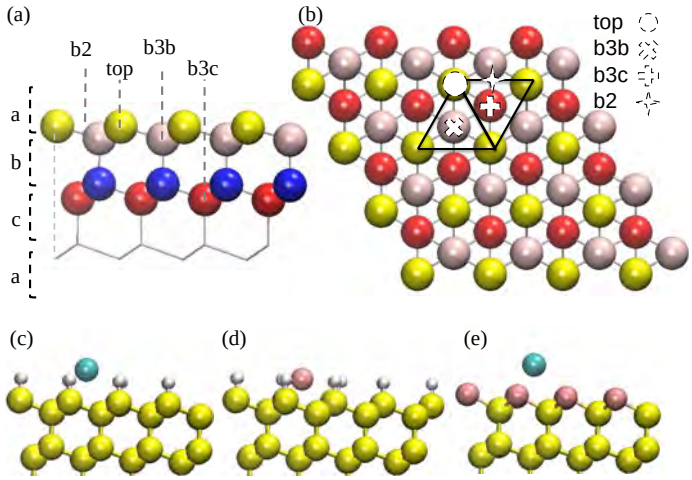


Figure 4.19 – *Density Functional Theory (DFT) calculations. (a) Side view and (b) Top view of the Si(111) slab used in the calculations where the investigated adsorption sites are shown: top, b2, b3b, b3c. The first to fourth layers are colored in yellow, beige, blue and red respectively in order to highlight repeating pattern observed in the layers stacking of (111) oriented Si crystal. (c) Adsorbed configurations of In on H-terminated Si(111):1x1 surface as resulted from HF treated surface. (d) Adsorbed configurations of As on H-terminated Si(111):1x1 surface. (e) Adsorbed configurations of In on As-terminated Si(111):1x1 surface as after an arsenic treatment. In (c), (d) and (e), yellow, white, cyan and pink spheres are respectively Si, H, In and As atoms. This color scheme is also used in 4.18.*

The adsorption of both In and As atoms, also called ad-atoms in the following, on H-terminated Si(111):1x1 have been performed likewise the adsorption of In ad-atom on As-terminated Si(111):1x1. Several initial positions for the ad-atoms have been tested as a function of the Si(111) topology and, taking advantages of the symmetry of the system, only the most favorable configurations are discussed in the following. The Top configuration corresponds to an ad-atom adsorbed above one atom of the topmost layer (either H or As atom as a function of the surface treatment). Two other configurations are discussed, where As or In atom can adsorb as a bridge configuration either between two atoms of the topmost layer (As or H species) referred as b2 adsorption site or between three atoms of the topmost layer, either As or H specie, and named b3b and b3c depending on the layer stacking of the silicon Si(111) substrate as schematized in figure 4.19(a) and figure 4.19(b) (with respect to the periodic abc-like stacking in the Si(111) substrate).

	H-terminated Si(111):1x1				*As-terminated Si(111):1x1*	
	As adsorption		*In adsorption*		*In adsorption*	
	E_{ads}*(ev)*	*d(As-H) (Å)*	*Eads (eV)*	*d(In-H)((Å)*	*Eads (eV)*	*d(In-As) (Å)*
Top					*-1.24*	*2.88*
b2	*-0.41*	*2.12*	*-0.83*	*2.55*	*Non-stable*	*-*
b3b	*0.73*	*2.70*	*-0.83*	*2.54*	*-1.58*	*3.15*
b3c	*0.33*	*2.70*	*-0.85*	*2.54*	*-1.60*	*3.17*

Table 4.5 – *Adsorption energy (Eads in eV) and typical bondlength (d in Å) for single As and In on H-term surface and Adsorption energy for single In on As-term surface.*

Adsorption energies and typical bond lengths are provided in table 4.5. For the adsorption of As and In atoms on H-terminated surface, the adsorption energies are endothermic or slightly exothermic for the most favored adsorptions [-0.85 eV for In adsorption figure 4.19(c)]. Note here that the adsorption of As ad-atom implies a deep deformation in the H atoms layer where H atoms are repelled from As atom to allow the ad-atom As to come closer to the underlying topmost layers of the Si substrate, revealing a favorable interaction between Si and As species [figure 4.19(d)]. Such a deformation of the whole system involves a significant deformation cost as revealed by the energetic penalty of the adsorption energy. These observations are consistent with the measured typical bond lengths on such adsorbed states which are larger than the ones from references calculations on simple molecules (like InH_3 and AsH_3) and from tabulated experimental data. Thus, the H atoms prefer to maintain a strong bond with the Si substrate and keep the ad-atoms far from the surface. To go further, we perform calculations to evaluate if In atom can adsorb on H-terminated Si(111):1x1 through more complex mechanisms involving H_2 or InH_3 desorption. Only the desorption of an InH_3 molecule associated to the subsequent adsorption of an In atom on the empty space "b3 site" left is a favorable exothermic process. Considering energetics of Table 4.5, such mechanism involving Si-H breaking must require a thermal activation. Investigating such reaction paths and associated activation barriers is beyond the scope of this study. This confirms that the adsorption reaction of both As and In on H-terminated surface is not favorable at low temperature. Thus, the hydrogen preparation of the surfaces, prior to growth, not only fills all dangling bonds, increasing the diffusion of elements III, but also prevents indium and arsenic incorporation at low temperature. Keeping "clean" surfaces, hydrogen allows to reduce the annealing temperature at which is formed the As-term Si surface.

In addition, in the case of the adsorption of In atom on As-terminated Si surface, large adsorption energies are observed favoring b3-type sites. Top configuration is also an observed adsorbed state which reveals to be metastable reaching b3-type configurations without any activation barrier [figure 4.19(e)]. DFT calculations highlight the favorable adsorption of In species on As-terminated Si(111):1x1, which is stabilized at the early stages of deposition as a bridge configuration. We also estimate the barrier energy for the adsorbed In atom on a b3 site to reach a nearby b3 site using NEB calculations. A very low activation barrier of 0.10 eV was obtained (or 0.35 eV when passing by top configuration), highlighting the ability of the In atom to migrate on the surface, which is favorable for the nucleation process.

4.5.4 Growths of InAs(Sb) nanowires on patterned Si wafers

Finally, growths were developed in patterns. Details on the patterning process can be found in Appendix E. Each patterned substrates is composed of hole arrays having a diameter of 40, 80, 100, 120, 150 and 200nm; and a pitch of 100, 200 and 500 nm. 15 growth environments are thus available on each wafer. The growth was carried out for 2 different flux parameters for both In (3.1 x$10^{-8}$and 6.2 x10^{-8}Torr) and As (1.2 x$10^{-5}$and 2.4 x10^{-5}Torr) keeping other growth parameters constant. The wafer degassing before growth was carried out at 200 °C for 1 hour with a H_2 plasma environment: 2 sccm flux of hydrogen (RF source and Power = 250 Watts). The arsenic treatment before growth was carried out for 20 minutes at 650 °C and hence the nanowires in the patterned wafers are no more CMOS compatible. Figure 4.20 presents SEM images of as-grown InAs nanowires on patterned substrates, which confirms a high vertical yield.

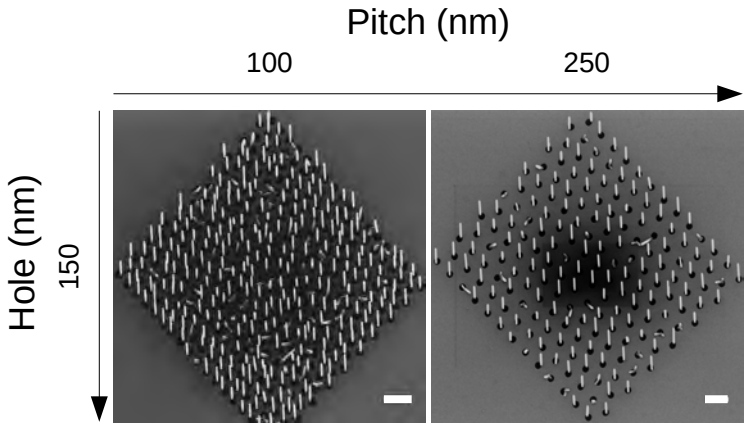


Figure 4.20 – *SEM images of InAs nanowires grown on patterned substrates. The pitch increases from left to right and the hole diameter from top to bottom. In flux is 6.2x10^{-8} Torr and As flux is 0.6x10^{-5} Torr. Scale bars are 500 nm.*

The figure 4.21 presents a statistical analysis of these growths as a function of the pattern parameters and the growth conditions. For each pitch, the vertical yield, the average diameter and the average length of InAs nanowires is reported for each growth condition (set of color). The analysis was carried out using the image and data treatment procedure presented and discussed in chapter 2. First, each nanowire array has been characterized thanks to SEM measurements and analyzed separately. Then, the vertical yield was determined by counting the number of fully vertical wires with respect to the total number of holes in the pattern. For each configuration, the average length and diameter were calculated on the fully vertical wires.

The first conclusion of these studies is that the vertical yield is above 80% in many case, which is encouraging for future devices. It is also clear that the yield improves when the In flux is high (Blue and Magenta), and specially for small hole diameters. Similarly, the nanowire diameter increases with the In flux for a fixed pattern configuration and with the hole diameter. This can be explained by a short indium diffusion length on SiO_2 compared to Si : higher In fluxes are necessary for growth in small holes and thicker wires are obtained when holes are larger. Moreover, the pitch seems to have a limited influence on the nanowire length, which can be explained by growth conditions that do not

lead to a diffusion limited regime. Finally, doubling both In and As fluxes is necessary for almost doubling the nanowire length, which can be explained by conditions near equilibrium: neither In or As are clearly limiting the growth rate.

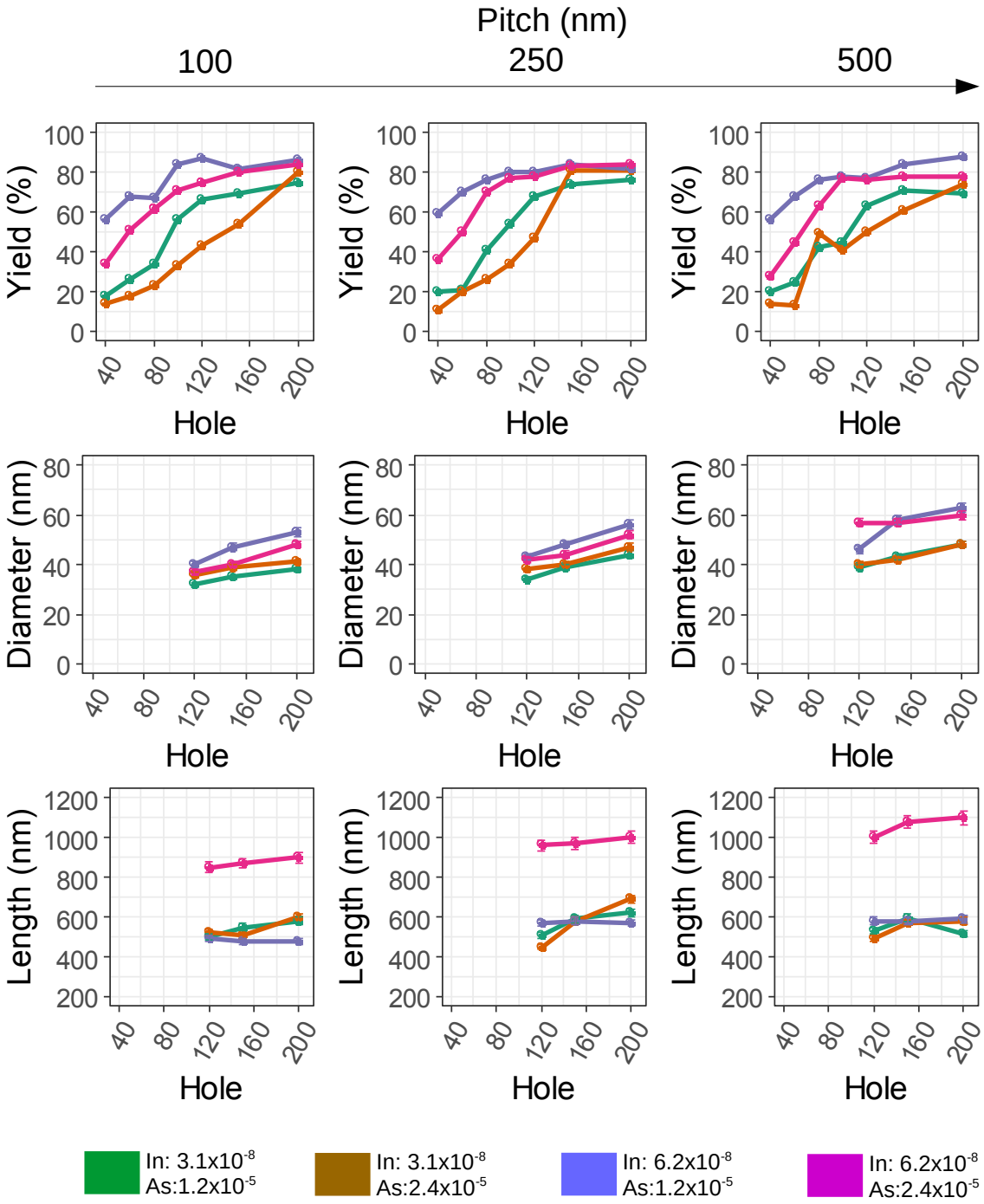


Figure 4.21 – *InAs nanowires on patterned Si(111). Each color corresponds to a specific set of growth conditions: (i.e. a specific In and an As flux). For each plot, the x-axis corresponds to the hole diameters and the y-axis to the vertical yield (top three plots), to the nanowire diameter (middle three plots) and to the length (bottom three plots). The pitch increases from left to right.*

The growth on patterned substrates was further extended to InAsSb nanowires having an Sb composition of 5 %. Three growth conditions were considered with In/As fluxes of $3.1x10^{-8}$/ $0.6x10^{-5}$; $6.1x10^{-8}$/ $1.2x10^{-5}$and $6.1x10^{-8}$/ $2.4x10^{-5}$Torr respectively. The figure 4.22 presents two SEM images of InAsSb nanowires grown in 200nm diameter holes and for which a high vertical yield is reported. Similarly that for InAs nanowire, statistics about the vertical yield, the nanowire length and the nanowire diameter are reported in figure 4.23.

It is interesting to note that, similarly to what is observed for InAs nanowires, the global behavior is the same: the yield improves when the In flux is high (specially for small diameter holes); the nanowire diameter increases with the In flux for a fixed pattern configuration and with the hole diameter. On the contrary, the nanowire length is clearly reduced due to the antimony surfactant effect, and the pitch starts to influence it; which could be explained by the appearance of a diffusion limited process in correlation with the antimony. Finally, when compared to InAs (figure 4.21), the Sb incorporation decreases the vertical growth rate, and thus the InAsSb nanowires tend to become fatter and shorter.

Advantages of InAsSb nanowires compared to InAs one are that the electron mobility is higher and that the crystalline structure can be fully ZB. However, to the date only few groups[263–267] have reported self-catalyzed and fully vertical InAsSb nanowires on Si. For instance, Sourribes et al.[267], integrated InAsSb on bare Si(111) in their MBE system and observed a sharp decrease in the stacking faults density when increasing Sb. Anyebe et al.[263,264] reported a significant surfactant effect of Sb that hinders the axial growth. To our knowledge, the growth of fully vertical and self-catalyzed InAsSb nanowires on patterned Si(111) wafers, despite full of positive promises from the material aspect, is still missing.

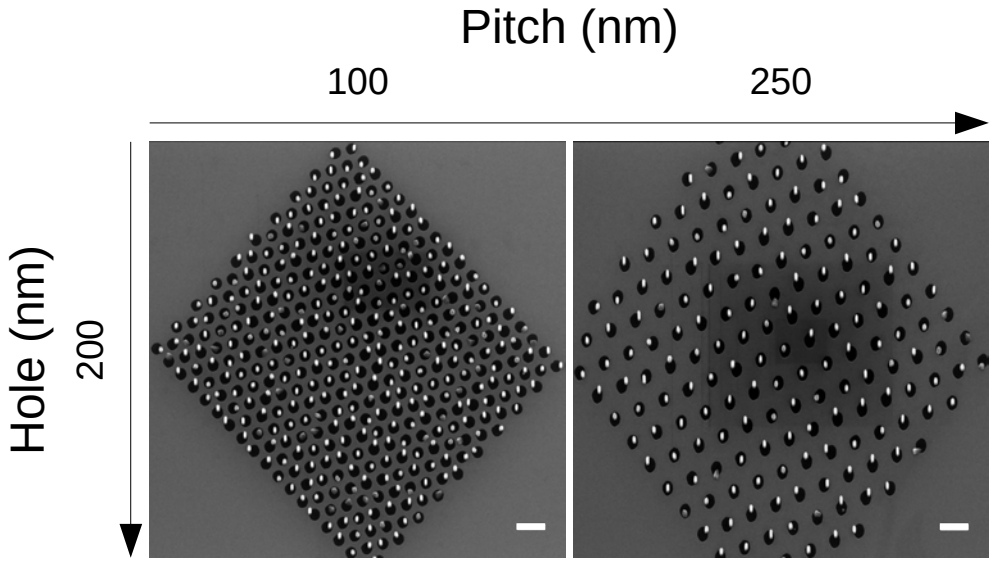


Figure 4.22 – *SEM images of as-grown InAsSb nanowires on a pattern substrate. The In Flux is $6.2x10^{-8}$ Torr, the As flux is $0.6x10^{-5}$ Torr and the Sb flux is $1x10^{-7}$Torr. The pitch increases from left to right. Scale bars are 500 nm.*

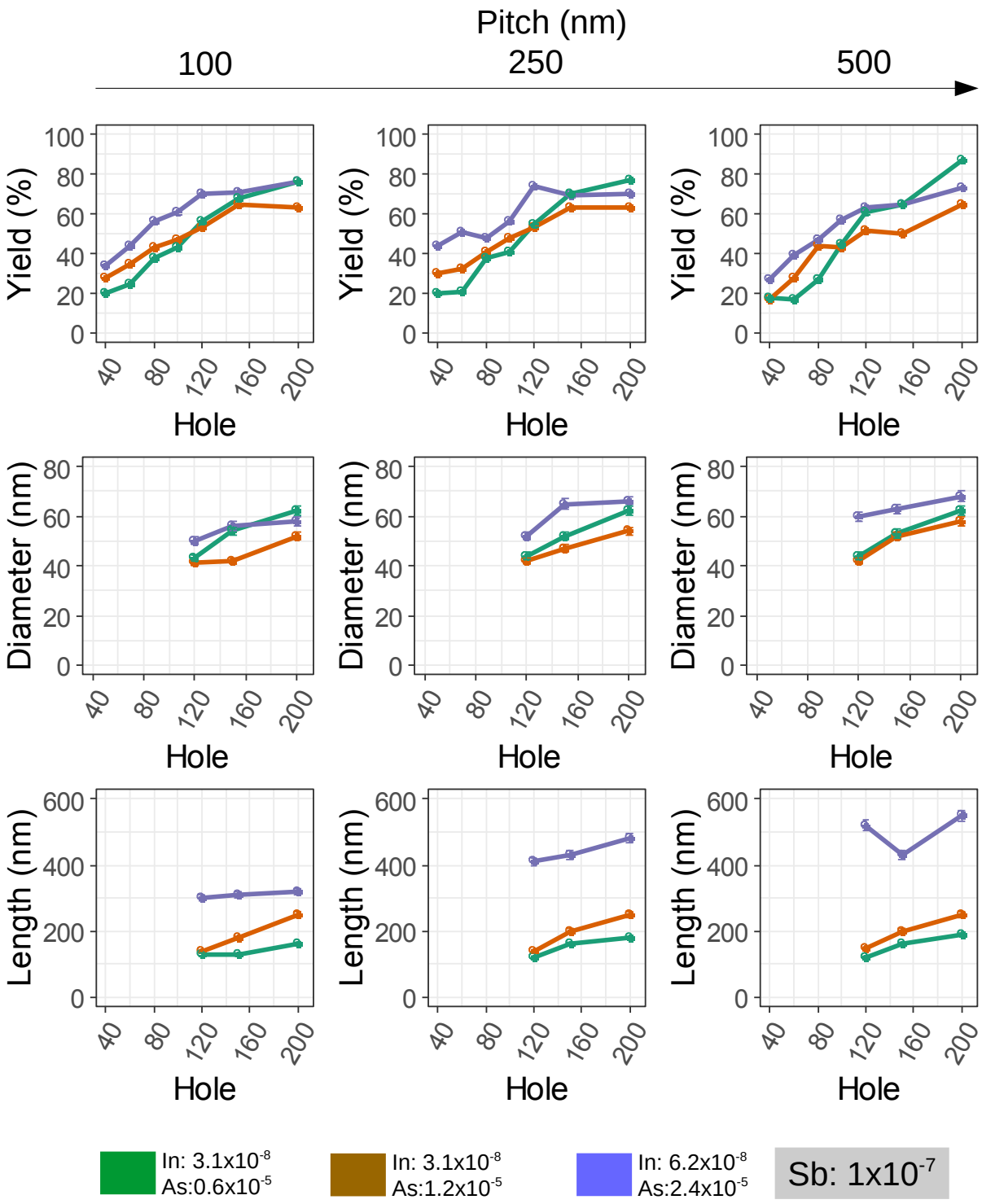


Figure 4.23 – *InAsSb nanowires on patterned Si(111). Each color corresponds to a specific set of growth conditions: (i.e. a specific In and an As flux). For each plot, the x-axis corresponds to the hole diameters and the y-axis to the vertical yield (top three plots), to the nanowire diameter (middle three plots) and to the length (bottom three plots). The pitch increases from left to right.*

4.6 Conclusion

InAs nanowires could represent an ideal building brick for future 3D transistors thanks to their high electron mobility, their integration on silicon and the pinning of the fermi level at their surface allowing to take ohmic contacts. However, full BEOL CMOS compatibility has not been reported yet since one of the following key ingredient is always missing: (i) full verticality on silicon, (ii) gold-free nanowire growth (either self-catalyzed or CMOS compatible catalyst) , (iii) thermal budget below 450°C.

The objective of this chapter was to systematically address those bottlenecks and develop a new process for CMOS nanowire integration. Our contribution was divided in two parts. The first one was focused on gathering the necessary surface treatment ingredients, allowing full vertical integration on silicon. For this reasons, we started by probing few key parameters in order to understand their influence on nanowire growth. It was found that a H_2 plasma treatment is optimum when the degassing temperature is low, there is no significant influence of the H_2 flux used during the degassing, and more importantly it was confirmed that the high temperature As annealing before growth can be converted to a low temperature one while keeping fully vertical nanowires. After reporting full CMOS compatible InAs nanowires, the thesis focused on the systematic study of the different surface preparations and the understanding of the possible chemical mechanism leading to different surface terminations.

Following, we proposed a process allowing the growth of fully vertical InAs nanowires on Si by MBE without crossing the 410°C growth temperature, which is compatible with the BEOL limitations. The "key" role of hydrogen during substrate preparation was presented and discussed in details from both experimental and theoretical point of view. A description of the different surface preparations was proposed and consequences on the nanowire growth are presented. The change from a VS to a VLS growth mechanism for self-catalyzed InAs nanowires was reported and explained by the surface diffusion of element III. These results further explain the differences observed between MBE and MOVPE growth of InAs nanowires on silicon leading to a better understanding of the nucleation mechanisms and the development of new processes involving hydrogen preparations. Finally, an unexpected difference between H_2-gas and H_2-plasma surface preparations was reported and related to surface termination. Overall, our results suggest a new method for surface preparation and a possible tuning of the growth mechanism using different surface terminations.

Finally, high yield of InAs and InAsSb nanowire arrays are reported on silicon. Although the arsenic annealing temperature before growth is above thermal budget and the wires are no more CMOS compatible, the same trend was observed than for unpatterned substrates: high In and high As lead to the growth of InAs and InAsSb having better aspect ratios (almost double).

In addition, our process allows the growth long and thin wires, which is favorable for 3D transistors. Indeed, in the nanoelectronics context, the nanowire diameter is a key parameter and should be inferior to 20nm for channel electrostatic control, which is easily achievable by reducing the growth

time (a diameter of 20nm for a length of 500nm). Moreover, InAs is the starting point of other complex structures such as InAs-GaSb core-shell TFETs. Finally, even if Si(001) is the industrial standard, it is possible to bond a Si(111) wafer ontop of a Si(001) one, thanks to a well-established industrial procedure: the SmartCut from Soitec. More details can be found in the website of Soitec (www.soitec.fr). The full BEOL CMOS compatibility is thus achievable, last bottlenecks being lifted.

Chapter 5

$Bi_{1-x}Sb_x$ Nanoscale 3D Topological Insulators for Quantum Computing

In computer science, computational approach refers to the way informations are stored and manipulated in the computer memory. It plays a key role in determining the processing speed, which can be improved either by increasing the transistor speed or by implementing parallel processing and mulithreading. A computer program is composed of series of instructions based on "0" and "1" strings, that run sequentially one after another. In the multithreading approach, the program is subdivided and assigned to different cores that run in parallel in the Central Processing Unit (CPU). The way of storing informations, either in "0" or "1" strings, is known as classical logic or Boolean one. This approach addresses almost all the consumer electronics needs, however it is inefficient when dealing with some complex scientific or mathematical problems; even with optimized algorithms and a maximal processing power. For instance, modern cryptography relies on very large prime numbers (~200 numbers in length) and even most advanced computers with well optimized algorithms encounter difficulties for gaining processing time.

Another possible approach is the to use quantum bits (Qubits) as proposed by Richard Feynman in 1981[268], in order to process informations. What was just a fundamental theory gathered attention in the 1990s, when two algorithms for quantum computers demonstrated exponential gains in the processing time: the Shors'[269] algorithm focuses on finding very big prime numbers, whereas the Grover's[270] one search for a specified entry in an unordered database. Similarly to "bits" for classical computers, Qubits are the basic building blocks of quantum computers. Contrary to classical "bits", they are built from a two state quantum system that can be "0" or "1" or both values at the same time. Moreover, Qubits benefit of two main principles of quantum mechanics: superposition and entanglement[271]. Examples of two state quantum mechanical systems are: polarization of light (horizontal and vertical), spin of electrons (spin-up and spin-down), ... etc.

Any two-level system can be used as a Qubit, which explains why their physical implementations are diverse: photons, electrons, nucleus, optical lattices, Josephson junctions, Quantum dots, etc. and based on diverse physical principles such as the polarization of light, the spin or the charge of electrons or atoms, etc ... One of the possibilities is to use Majorana fermions (Mfs) implemented

in hybrid interfaces for creating topologically protected Qubits[272]. Majorana fermions are fermionic particles solving the Majorana equation[273]. They are particles, which are their own antiparticles, and thus are neutral, spin $-\frac{1}{2}$ particle, and their field equations are invariant to charge conjugation. Since 2012, different groups report on the Majorana fermions implementation in hybrid interfaces between a superconductor (Al, NbN), and a high electron mobility III-V nanowire such as InAs[274] and InSb[275]. The fundamental reason for choosing these materials is their strong spin-orbit (S-O) interactions, which is one of the key ingredient for creating MFs. In the meanwhile, the discovery Topological Insulators (TIs)[276,277] completely changed our vision of condensed matter: "A topological insulator is a material with non-trivial symmetry-protected topological order that behaves as an insulator in its interior but whose surface contains conducting states"[278]. These conducting states are topologically protected from environment and can host robust Majorana fermions[279]. This makes TI nanowires appealing for implementing topological Qubits in condensed matter. In this context, the development of new nanoscale Topological Insulators grown by cutting edge techniques such as Molecular Beam Epitaxy (MBE), which is known for growing highest quality crystals, is essential.

On the material side, TIs are mostly based on the bismuth family and bismuth antimony alloys ($Bi_{1-x}Sb_x$)[280] were the first experimentally confirmed 3D TI in 2008. In the following, our goal is to integrate $Bi_{1-x}Sb_x$ nanowires, with controlled Sb composition, on silicon by Molecular Beam Epitaxy (MBE). The chapter starts with a brief Qubits overview and then material aspects are developed. Next, the nanowire based topological Qubits and the 3D topological insulators are presented. Finally, our contribution to the field is presented including direct growth of $Bi_{1-x}Sb$ nanowires on silicon, the control of the Sb composition, the full structural characterization of these nanostructures and few other advanced characterizations. The chapter ends with conclusions and outlooks.

5.1 The Qubits

The figure 5.1 presents a scheme comparing a classical bit on the left and a Qubit on the right (on the Dirac Sphere). Whereas the two possible states of a bit are "0" or "1", the general quantum state of a Qubit can be represented by a linear superposition of its two basis states $|0>$and $|1>$ (pronounced "ket-0" and "ket-1", respectively in the Dirac or Bra-ket notation). The system can be described by the linear combination of both as: $|\psi>=\alpha|0>+\beta|0>$, where α and β are the complex probabilistic amplitudes. Using the Bloch sphere representation (figure 5.1), the north and south poles of this sphere are defined as $|0>$ and $|1>$ respectively. For classical bits, apart from this two poles the rest of the sphere is forbidden. In contrast, for Qubits, the principle of superposition permits to take any position in the sphere, and similarly, the entanglement allows a set of Qubits to express higher correlations: i.e. taking multiple states at the same time. Moreover, since a n Qubit register can have 2^n states simultaneously, an exponential increase in processing speed can be observed when the value of n increases (compared to classical bits). Mathematically, a n Qubit system can be expressed as :

$|\Psi_n>=\sum_{i=0}^{2^n-1} a_i|i>$where i is an integer and $\sum_{i=0}^{2^n-1} a_i|i|^2=1$.

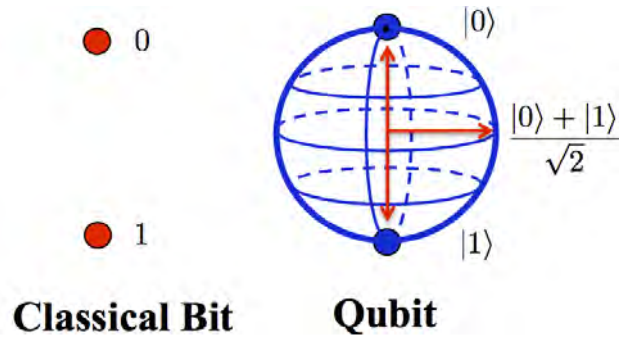


Figure 5.1 – *Bloch Sphere. Image Source (http://qoqms.phys.strath.ac.uk/figures/qubit.png)*

5.2 Materials for Qubit implementation

The figure 5.2 lists different candidates for Qubits implementation in condensed matter. This is based on a review published in a special issue of the Materials Research Society journal "Materials issues for quantum computation" (Volume 38 - Issue 10 - October 2013), that can be found in references[281–285].

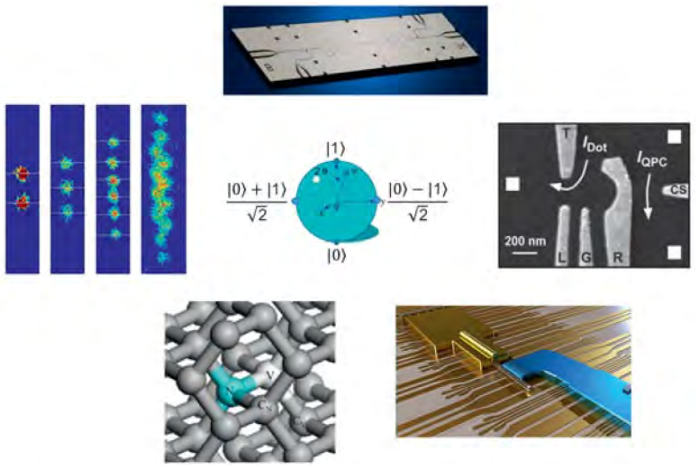


Figure 5.2 – *List of the different candidates for Qubits implementation in condensed matter. A Qubit (in the center) can be induced in a wide range of material systems. Clockwise from top are presented: superconducting resonators and Josephson junctions, SiGe gate-defined spin Qubits, Majorana fermions in superconductor/semiconductor nanowire hybrid materials, spin defects in solids, and hyperfine states in trapped ion systems. (Eckstein et al.[281])*

In the following, a brief overview for each of them is presented:

1. **Superconducting resonators and Josephson junctions:** "Superconducting qubits are lithographically fabricated electrical circuits comprising inductors, capacitors, Josephson junctions, and interconnects"[283]. They are based on Josephson tunnel junction, which is a weak link between two superconductors, and thus allows electron tunnelings. When the system is close to 0K, it behaves like a mechanical "artificial atom" exhibiting quantized states of electronic charge, magnetic flux or junction phase depending upon the design. A charge Qubit

consists in a superconducting island coupled to a superconducting reservoir by a Josephson junction. This Qubit is controlled by a tension that can induce charge differences between both sides of the junction. On the other hand, in the flux Qubit, a superconducting loop of inductance L is interrupted by a Josephson junctions. When a magnetic filed is applied to the superconducting loop, a current is induced. Finally, a phase Qubit is fabricated with current biased Josephson junctions[283].

2. **Gate-defined spin Qubits:** "One of the most powerful approaches to solid-state quantum computation involves the use of two-dimensional electron gases that are gated so as to confine single electrons and their spins." It was first proposed by Loss and DiVincenzo[286,287] for the GaAs system and is now implemented in GaAs/AlGaAs[288] and Si/SiGe[289] heterostructures. It is possible to implement charge or spin Qubits in these structures. The charge Qubit is formed by tuning the back-gate voltage so that only one electron or hole can enter in the quantum dot. The spin Qubit can be implemented thank to the Zeeman energy splitting of spin-up and spin-down electrons.

3. **Majorana fermions in superconductor/semiconductor nanowire hybrid interfaces:** Hybrid interfaces consisting of a semiconducting nanowires with strong spin-orbit interactions (i.e.: InSb[275] and InAs[274]), and a superconductor can host Majorana fermions. In a topological Qubit, the location of the Majorana fermions is the quantum variable, and processing information consists in moving Mfs. To realize topological Qubits, three ingredient are needed: a semiconducting nanowire with strong orbit interactions (SOI), a superconducting material and an external magnetic field.

4. **Spin defects in solids:** Defects in certain crystals, like nitrogen vacancy centers in diamond[290,291], di-vancancy in SiC[292,293] etc., can host quantized states when probed with optical and microwave excitations and electric and magnetic fields. It is thus possible to create spin Qubits in these materials if: (i) the material is a crystalline and paramagnetic to support energy splittings, (ii) it is a wide band gap material to accommodate deep centres, (iii) it has small spin orbit interactions in order to avoid spin flips, (iv) the material is of high quality to avoid paramagnetic imperfections and (iv) ideally with zero nuclear spins.[285]

5. **Hyperfine states in trapped ion systems:** "Electromagnetic confinement of individual ions ("ion traps") represents a highly promising approach to the development of quantum information technology. Here, the quantum state is a combination of the hyperfine electronic state of the ion and its center-of-mass motional state". In an ion trap[294,295], four electrodes provide a confining force to keep the ions nearly on-axis, thanks to an ac voltage. A fixed positive voltage is implemented on the other side of the trap to prevent escape in the z direction. When the trapped ions are cooled down, quantum information is contained in the superposition of two hyperfine states chosen to be '0' and '1'.

5.3 Topological qubits in 1D hybrid systems

Majorana fermions are mathematical solutions of the Majorana equation. They are fermions that are their own antiparticle, and thus have zero charge and are neutral spin-1/2 particles. Up to now the particle existence is not reported in nature, but, in condensed matter physics, bound Majorana fermions can appear as quasiparticle excitations. They are governed by non-abelian statistics, always appear by pairs and can be used as topological Qubits in quantum computers. The first proposal for implementing Mfs in condensed matter was reported by Alexei Kitaev[296], when he suggested that Majorana particles should emerge in condensed matter systems as zero mode excitations in one-dimensional p-wave superconductors. The first realistic recipe for creating Mfs was subsequently proposed: creating artificially a one-dimensional p-wave superconductors based on a semiconductor nanowire with high spin-orbit interactions, induced superconducting s-wave pairing and Zeeman splitting. These necessary ingredients were combined for the first time by Mourik et al.[275]:

1. High quality InSb nanowires. The strong spin orbit interactions in InSb not only suppresses spin freedom degrees but also assists in closing the gap.

2. A NbTiN S-wave superconductor is deposited ontop of the InSb nanowires and induces pairing in the nanowire between electron states of opposite momentum and opposite spins. It also induces a gap Δ.

3. The Zeeman splitting is realized thanks to a magnetic field applied along the nanowire axis. The gap can be opened at the crossing point between the two spin orbit bands. The degeneracy is two fold if the Fermi energy is inside this gap, fourfold otherwise.

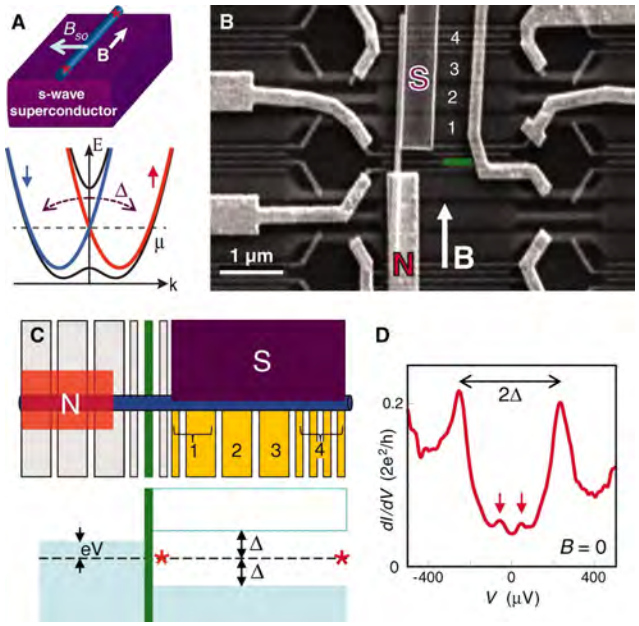


Figure 5.3 – *Signatures of Majorana Fermions in InSb Nanowires Source: Mourik et al.*[275]

Based on these three ingredients, the two fold degeneracy, when coupled with Δ, creates a topological superconducting phase with $E_z \geq \sqrt{\Delta^2 + \mu^2}$, where E_z is the Zeeman energy and can be expressed as $E_z = g\frac{\mu_B B}{2}$ where g is the Landé g-factor and B is the Bohr magneton. Interestingly, when $E_z = \sqrt{\Delta^2 + \mu^2}$, pairs of Majorana bound states can arise at zero-energy; one at each end of the wire. In the paper[275] published by a group from TU Delft, signatures of Majorana fermions in an InSb nanowire half-covered by a Niobium Titane Nitride (NbTiN) electrode (s-wave superconductor) were reported in 2012 at 0.15 K (figure 5.3). The same year a group from Lund University led by prof H.Q Xu[297] also reported Majorna Fermion using InSb nanowires and Nb s-wave superconductor, and a group from the Weizmann Institute of Science, Israel[298] used InAs nanowires with Al superconducting contacts to host Majorana fermions.

Despite fascinating properties, the implementation of Majorana fermions for creating topological Qubits in an industrial environment faces two major bottlenecks. First, the temperature at which Majorana fermions have been reported is very low. Secondly, the external magnetic field needed to create the Zeeman splitting is extremely high and weaken the induced superconducting gap. While the temperature is related to the nature of superconducting material used, the amount of magnetic field is related to a 1D material that hosts Majorana fermions. The issue of magnetic field can be solved by changing the 1D semiconducting nanowire to a 1D 3D Topological Insulator. The next section presents these new materials.

5.4 3D Topolgical insulators

Topological Insulators (TIs) are a new class of materials that are electrical insulators in the inside and conduct electricity on the outer surface. In a 3D TI, the 3D bulk insulating band structure guarantees the protection of the 2D conducting surfaces, which are topologically protected by symmetry. This means that the surface states cannot be destroyed by non-magnetic impurities or imperfections, as schematically shown in figure 5.4. These topologically protected surface states are the consequence of two quantum mechanics features: the Time Reversal Symmetry (TRS) and the Spin-Orbit Interactions (SOIs)[299]. The TRS conservation implies that electron circulation in two opposite directions is equally realizable and the SOI represents the relativistic interaction between the electron's magnetic dipole, its orbital motion, and the electrostatic field of the positively charged nucleus. The heavier the element, the stronger SOIs are.

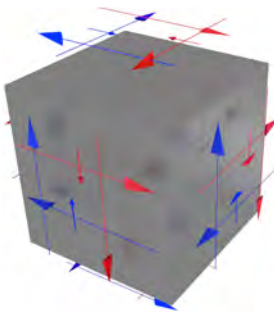


Figure 5.4 – *3D Sketch of a 3D Topological Insulator. The long arrows represent the momentum while small arrows represent the spin.*

In a Topological Insulator, carriers have their spin locked at a right-angle to their momentum (spin-momentum locking), which means that at a given energy, the only other available electronic states have different spin. This strongly suppresses carrier scattering and conduction on the surface is highly metallic. Figure 5.4 presents a sketch of a 3D Topological Insulator, in which the insulator bulk is represented by the cube, and the blue and red arrows represent the electron motion of opposite spin.

3D TIs were first proposed theoretically by Fu and Kane[276,277] from University of Pennsylvania in 2007, and measured experimentally one year later by a group of scientists led by Prof. Zahid Hasan from Princeton University[280]. 3D TIs, giving 2D conducting surface states, can be characterized by their Z_2 Topological Number having 4 parameters (v0;v1,v2,v3). If v0=1, the TI behavior is considered as "strong", whereas if v0=0, it is considered as a weak TI[300]. The geometry of the Fermi surface is strongly restricted by the Z_2 number just as the parity of Fermi surfaces number between two Time Reversal Invariant Momenta (TRIMs)[300].

From the material point of view, $Bi_{1-x}Sb_x$ alloys were the first experimentally confirmed 3D TI[280] and as presented in figure 5.5, the Angle Resolved Photo Emission Spectroscopy (ARPES) measurements on the $Bi_{1-x}Sb_x$ (111) surfaces confirms the Fermi level crossing the Dirac point an odd number of times. Similarly, the topological behavior and the gapless surface states are demonstrated for (110) surfaces by Zhu et al.[301]; and the suppression of backscattering by Roushan et al.[302] for (111) facets. However, despite these early achievements, the small band gap (0.03eV) of $Bi_{1-x}Sb_x$ and its complex band structure present experimental difficulties for bulk materials.

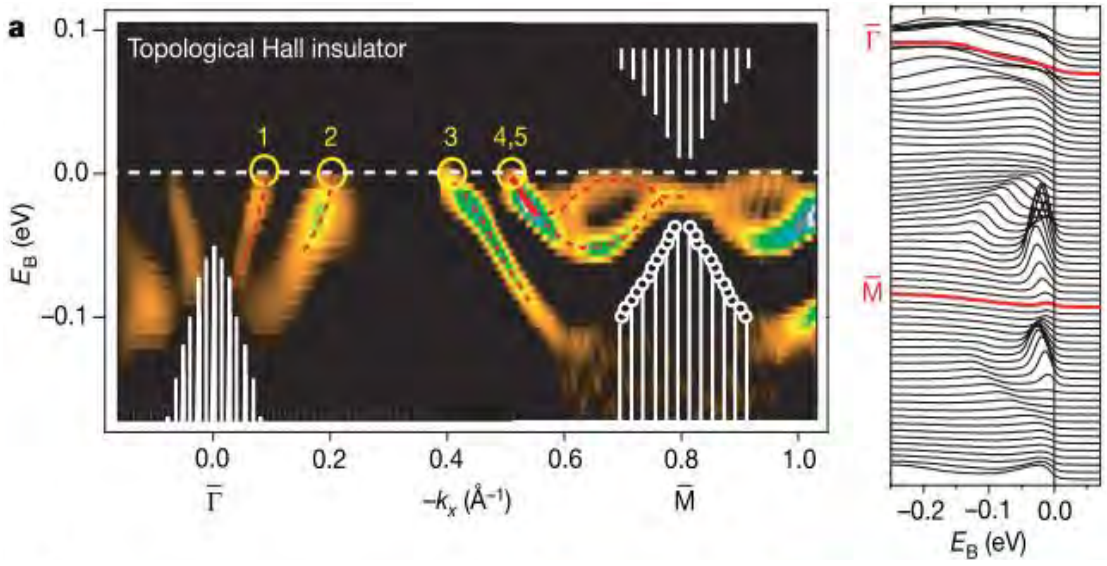


Figure 5.5 – *First experimental confirmed 3D topological insulator. Image Source:Hsieh et al.*[280] *"Angle-resolved photoemission spectroscopy (ARPES), is a direct experimental technique to observe the distribution of the electrons (more precisely, the density of single-particle electronic excitations) in the reciprocal space of solids. The technique is a refinement of ordinary photoemission spectroscopy, studying photoemission of electrons from a sample achieved usually by illumination with soft X-rays. ARPES is one of the most direct methods of studying the electronic structure of the surface of solids."*[303]

A second generation of strong 3D TIs was then studied including : Bi_2Se_3[304], Bi_2Te_3[305] and Sb_2Te_3[306]. These materials, previously known for their good thermoelectric properties[148,307–311], have the advantage of having larger band gaps (the Bi_2Se_3 band gap is 1.5eV[304]) and simpler surface states with a single Dirac cone on (111) surfaces[312]. Because of these advantages and since an external doping is possible, this second generation of 3D TIs gathered more and more attention. For instance Sb doping of Bi_2Se_3[313] and Bi_2Te_3[314] allows to control the carriers and the Fermi level. On the other hand, In doped Bi_2Se_3 materials[315] exhibits a metal to insulator transition. A complete list of theoretical and experimental studies related to 2D and 3D TIs was recently published by Bansil et al.[312].

5.4.1 The TI Nanostructures

As presented in section 5.4, replacing the 1D semiconductor by a nanoscale 3D Topological Insulator would be advantageous for realizing topological Qubits. Here, the bottleneck is to keep the TI behavior at nanoscale with the nanowire geometry. Luckily, the synthesis of defect free nanostructures (wires, flakes, ribbons, trees etc) was largely reported in the last decade; but, in our knowledge, only one group recently demonstrated the synthesis of nanoscale 3D TIs: Bi_2Se_3[12] and Bi_2Te_3 nanostructures[316] (wires, ribbons and flakes). In both cases, the growth system is a MOVPE reactor and gold is used to promote cracking of the metal organic precursors (figure 5.6 and 5.7). Due to the low growth temperature (incorporation of carbon) and the presence of gold, the residual doping level in these materials is expected to be important, which could reduce their TI behavior. Here, we propose to grow gold-free nanostructures in a MBE system in order to achieve highest quality of nanoscale materials.

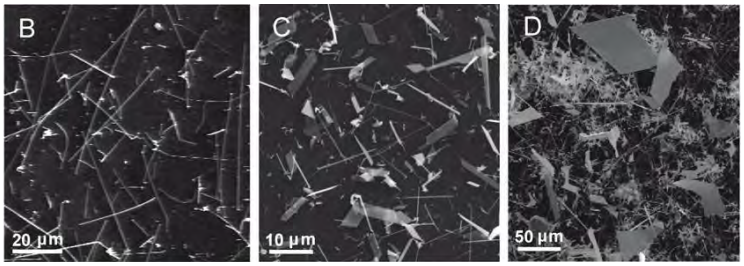


Figure 5.6 – *Synthesis of Bi_2Se_3 nanostructures by MOVPE. (Alegria et al.[12])*

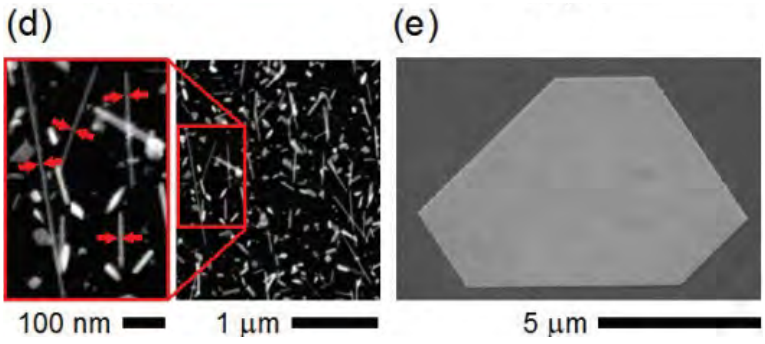


Figure 5.7 – *Synthesis of Bi_2Te_3 nanostructures by MOVPE. (Alegria et al.[316])*

5.5 The $Bi_{1-x}Sb_x$ alloys

Bi and Sb are heavy elements of the V_A column of the periodic table. The crystalline structure of Bi, Sb and $Bi_{1-x}Sb_x$ alloys is rhombohedral and their space group is $r\bar{3}m$ (N° 166) (see figure 5.8)[317]. The lattice structure can be easily understood in terms of two inter-penetrating face centered cubic (FCC) sub-lattices elongated along the trigonal direction of the FCC diagonal [figure 5.8 (a)][317]. Contrary to III-V materials, bismuth and antimony atoms are interchangeable in the matrix since they are both group V elements. Because of the C3 symmetry of the trigonal axis, the hexagonal coordinate system is generally preferred compared to the Cartesian one. In that case, the trigonal axis, the binary axis and the bisectrix axis of the crystal are denoted, respectively, by $[0001]$, $[1\bar{2}10]$ and $[10\bar{1}0]$ as shown in figure 5.8 (b) . The lattice constant of $Bi_{1-x}Sb_x$ change monotonically with the antimony composition x from pure Bismuth to pure Antimony (note here that there is no miscibility gap in the alloy)[317].

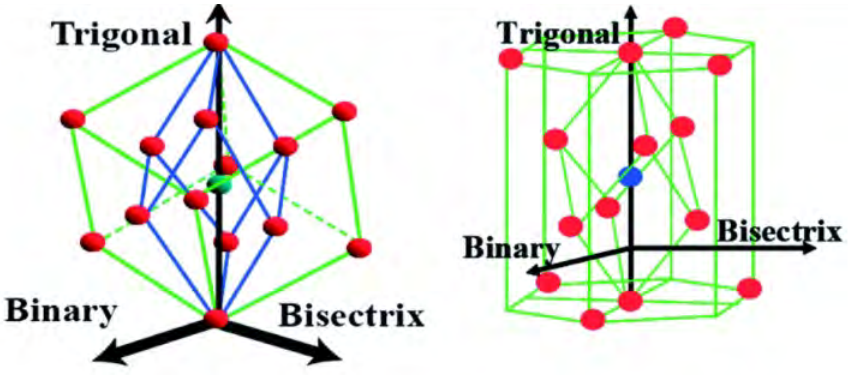


Figure 5.8 – *Crystalline structure of the $Bi_{1-x}Sb_x$ alloys. (Tang et al.[317])*

Sb (%)	a	c
100	4.3085	11.2732
95	4.3198	11.3195
90	4.3313	11.3588
85	4.3427	11.3945
80	4.3542	11.4282
75	4.366	11.4605
70	4.3772	11.4906
65	4.3887	11.52
60	4.4	11.548
55	4.412	11.576
50	4.4242	11.6037

Sb (%)	a	c
50	4.4242	11.6037
45	4.436	11.631
40	4.4483	11.6585
35	4.4605	11.6846
30	4.473	11.7105
25	4.4855	11.736
20	4.4978	11,7615
15	4.51	11.7867
10	4.5225	11.812
5	4.5347	11.8365
0	4.5465	11.8616

Table 5.1 – *Lattice parameters of the $Bi_{1-x}Sb_x$ alloys as a function of the Sb composition. Note that b=a. (Dismukes et al.[318])*

The figure 5.9 presents the electronic band structure of $Bi_{1-x}Sb_x$ alloys as a function of the antimony composition. It is suggested to behave as: a semi-metal (x<0.07), an indirect bandgap semiconductor (0.07<x<0.09, a direct bandgap semiconductor (0.09<x<0.15), an indirect bandgap semiconductor (0.15<x<0.22) and again semi-metal (x>0.22)[280,319] depending of the x composition. Consequently, a precise control of this parameter hold promises for future quantum devices. For instance, if x=0.03, 3D Dirac cones should be observed in the structure and could be used to host Majorana zero mode when coupled with a superconducting contact[276,280]. If 0.08<x<0.24 the material behaves as a 3D-topological insulator, and for x>0.23, the high electron mobility and strong spin-orbit interactions make it an interesting candidate for spintronics. Hence, excellent quality of 1D and 2D nanostructures, with controlled Sb compositions, is necessary in order to understand and engineer the material.

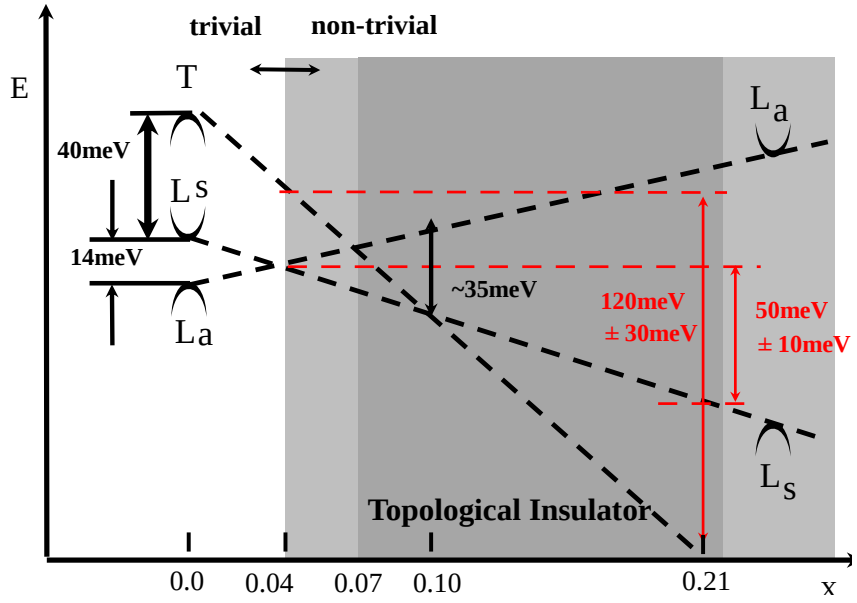


Figure 5.9 – *Band diagram of the $Bi_{1-x}Sb_x$alloys. Image Source: Nakamura et al.*[319]

5.6 My Contribution

5.6.1 First growths

The MBE nanowire synthesis is governed by few parameters that can be listed as: (i) the flux of each element present in the alloy, (ii) the growth temperature, and (iii) the growth time. As presented in chapter 3, the most influential parameter for growth is the temperature. Our first experiments were thus focused on determining a growth window for $Bi_{1-x}Sb_x$ alloys, by keeping both Bismuth and Antimony fluxes constant and equal, and then varying the temperature. If temperature is too low, a 2D bulk growth is obtained and if temperature is too high, everything is evaporated and no material deposition occurs. Once the temperature window is determined, the other aforementioned parameters are then adjusted according to the needs such as the morphology, the density, the composition, the growth direction ... etc.

After a quick literature search[148,149,317,319–322], and considering that both Bi and Sb are heavy elements, and thus are grown at low temperatures, we defined a set of three growth temperature: 100 °C, 200 °C, and 300 °C. Both bismuth and antimony fluxes are fixed at $1x10^{-7}$ Torr [Beam Equivalent Pressure (BEP)] and the growth time is 1 hour. For these initial growths, commercially available 2 inch Si(111) wafers from Siltronix were chemically deoxidized (HF 5% - 1 minute), immediately loaded into the MBE-412 system and finally degassed at 300°C for one hour. Samples were then transferred into the growth chamber and temperature was immediately raised to the growth conditions. The $Bi_{1-x}Sb_x$ growth was initiated and terminated by opening and closing both Bi and Sb shutters at the same time.

The figure 5.10 presents the SEM images of these initial trials. As expected, a 2D thin film growth is observed at low temperature [100°C - figure 5.10(a)], almost no material is deposited at high temperature [300°C - figure 5.10(c)]. On the contrary, nanocrystals are observed at 200°C [figure 5.10(b)], which suggests a growth window around this temperature.

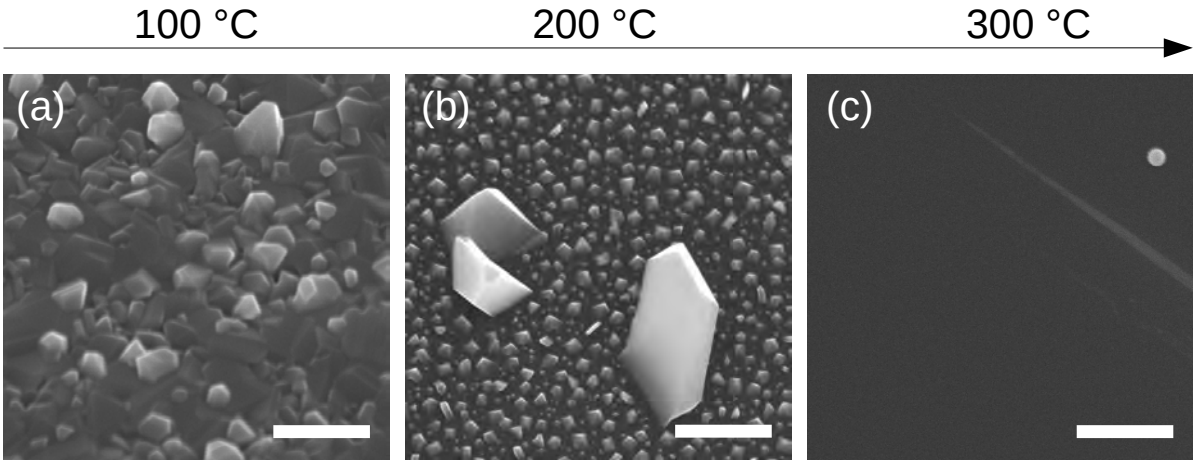


Figure 5.10 – *Determination of the growth window on Si(111). Bi and Sb fluxes are $1x10^{-7}$ Torr. The growth temperature increases from the left to the right. Scale bars are 500 nm.*

5.6.1.1 First nanostructures

Following these three initial trials, and considering a possible growth window ranging from 150°C to 250°C, the influence of the Sb flux was probed. The three next growths were carried out varying the Sb flux from of 0.25 to 0.5 and to $0.75x10^{-7}$ Torr while keeping a fixed Bi flux of $1x10^{-7}$ Torr. The growth temperature is fixed at 235 °C for 1 hour. Considering the lack of epitaxial relationship between the BiSb nanostructures and the Si(111) substrates, we now use deoxidized 2 inch Si(001) wafers from Siltronix. The other growth and characterization processes are the same as before. The figure 5.11 shows SEM images of these samples and interestingly different nanostructures including nanowires are present for all growth conditions. Additionally, it is worth to note that the density of nanostructures is lower when the Sb flux is low suggesting that a minimum Sb flux is needed to help the nucleation process.

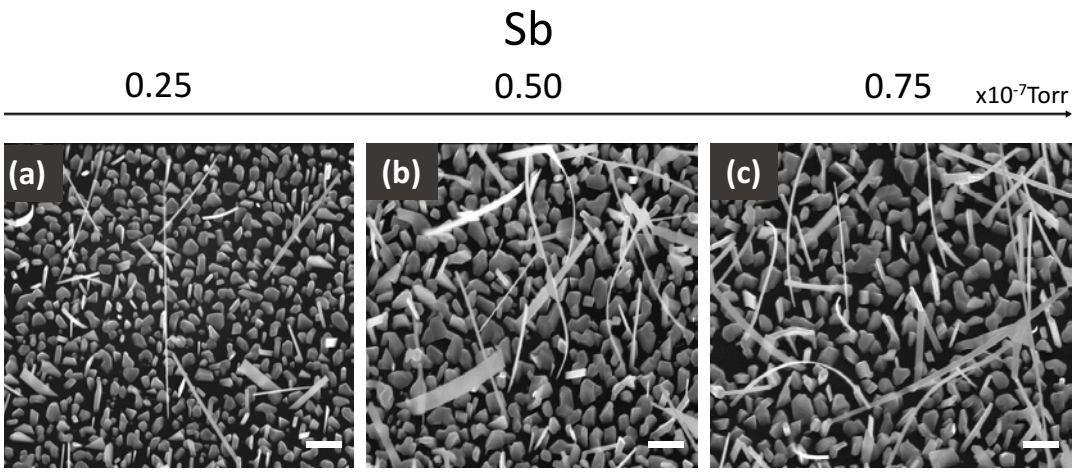


Figure 5.11 – *SEM images of our first $Bi_{1-x}Sb_x$ nanostructures on Si(001). The Bi flux is $1x10^{-7}$ Torr and Sb flux increases from left to the right. The growth temperature is 235°C, and the growth time is 1 hour. The SEM images were taken at a tilt angle of 30°. Scale bars are 500 nm.*

5.6.1.2 Nanoscale Geometry

In order to determine the morphology of the nanostructures grown in figure 5.11, we mechanically transferred the figure 5.11(b) sample onto a Si/SiO_2 substrates. Top view SEM images of the transferred nanostructures are presented in figure 5.12. Three nanoscale morphologies are present on this sample: the first one is nanowires, which are long and thin as reported in figure 5.12(b). The nanowire length can be up to 20µm for a diameter under 20nm, which lead to enormous aspect ratios. The second morphology is nanoribbons, which are long and large in one direction [figure 5.12(c)] . The third one is nanoflakes, which are very thin but extend in both x and y directions [figure 5.12(d)]. Both ribbons and flakes are so thin that it is possible to see through in the SEM [see figure 5.12(d)].

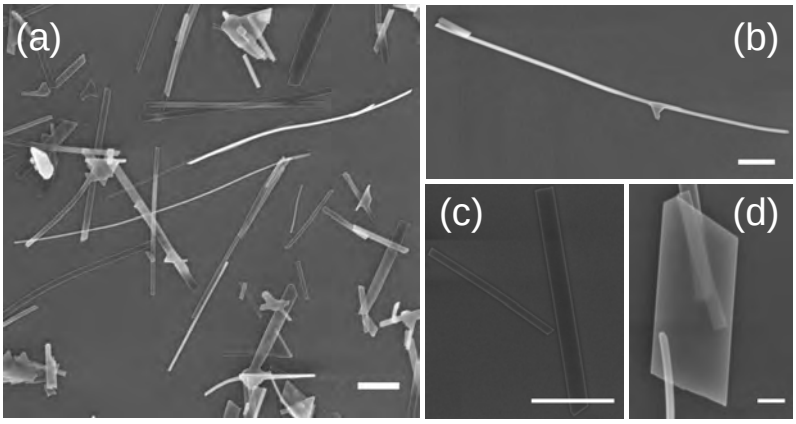


Figure 5.12 – *$Bi_{1-x}Sb_x$ nanstructures of figure 5.11(b) transfered on a Si/SiO_2 substrate. (a) global view, (b) a nanowire, (c) a nanoribbon and (d) a nanoflake. SEM images are top views. Scale bars are 500 nm.*

The observation of nanowires, nanoflakes and nanoribbons is particularly interesting for future quantum devices, and, at this stage, the first objective is achieved: the synthesis of new nanoscale $Bi_{1-x}Sb_x$ materials. Before exploring further the influence of the epitaxial parameters, the crystalline quality of these nanostructures needs to be assessed. The next three subsections present a complete TEM study of these nanostructures.

5.6.1.3 Structural Characterizations

The structural investigation of nanowires, corresponding to figure 5.12(b) growth conditions, was carried out by TEM. They were mechanically transferred on a carbon holey grid and their crystalline structure was analyzed by High Resolution TEM, using a JEOL 2100F having a field emission gun. The figure 5.13 presents TEM images, with corresponding Selected Area Electron Diffraction (SAED) patterns, of a single $Bi_{1-x}Sb_x$ nanowire in three different zone axis. First the nanowire is characterized in the <0001> zone axis [figure 5.13(a)]. The stage is then rotated of +32° [figure 5.13(b)] and -27° [figure 5.13(c)] around the growth direction, which correspond to the <-1101> and the <3–304> zone axis, respectively. The nanowire growth direction is [11-20] in the hexagonal coordinate system, which correspond to the [110] direction in the cubic coordinate system. After analysis, we confirmed that the crystalline structure is rhombohedral, and that $Bi_{1-x}Sb_x$ nanowires are defect-free and single crystalline nanostructures, which proves the high material quality. Note here that, during the thesis, more than 30 nanostructures were characterized by TEM and all of them were defect-free and single crystalline.

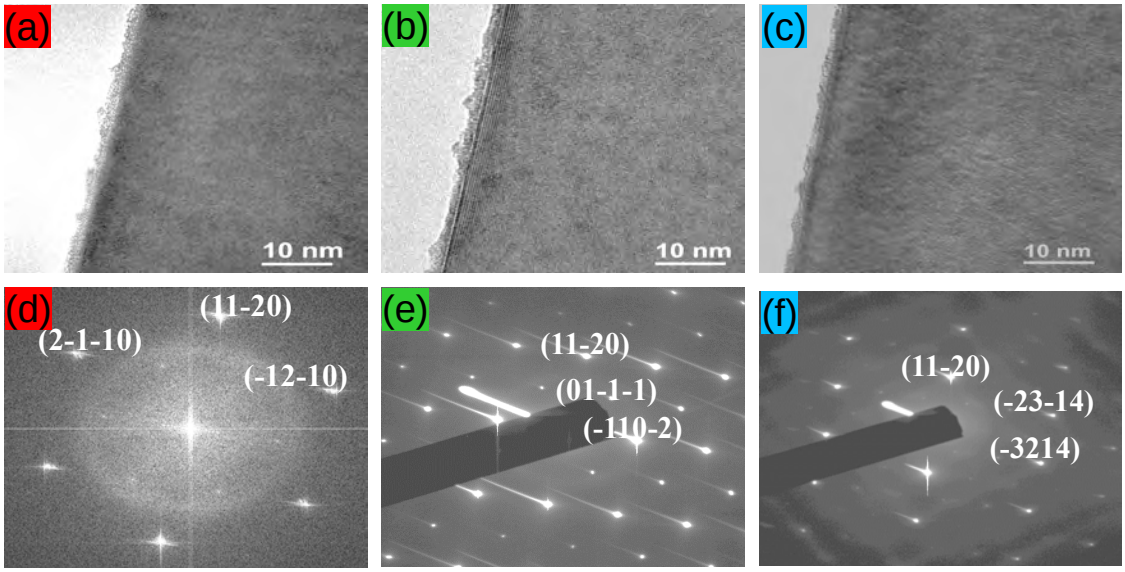


Figure 5.13 – *TEM characterization of a $Bi_{1-x}Sb_x$ nanowire. (a) HR-TEM image corresponding to the <0001> zone-axis, (b) HR-TEM image of the same nanowire rotated +32° around the growth direction and (c) HR-TEM image of the same nanowire rotated -27° around the growth direction. (d), (e) and (f) are SAED patterns of (a), (b) and (c) respectively.*

Further TEM measurements are presented in figure 5.14 (a-f) for different magnifications. While low magnification TEM images [figure 5.14 (a and b)] present the general nanowire morphology, high magnification ones [figure 5.14 (e and f)] provide information about atomic arrangements in the crystal. Once again, the structure is defect-free and single crystalline, but a native oxide is formed around the nanowire. This is not surprising since this wire was exposed to the ambient environment for a few weeks. This further suggest that high quality $Bi_{1-x}Sb_x$ nanowires should be stored in an UHV environment or in a controlled neutral one. It is also possible to embedded the nanowires in metallic arsenic for further STM or NanoARPES measurements.

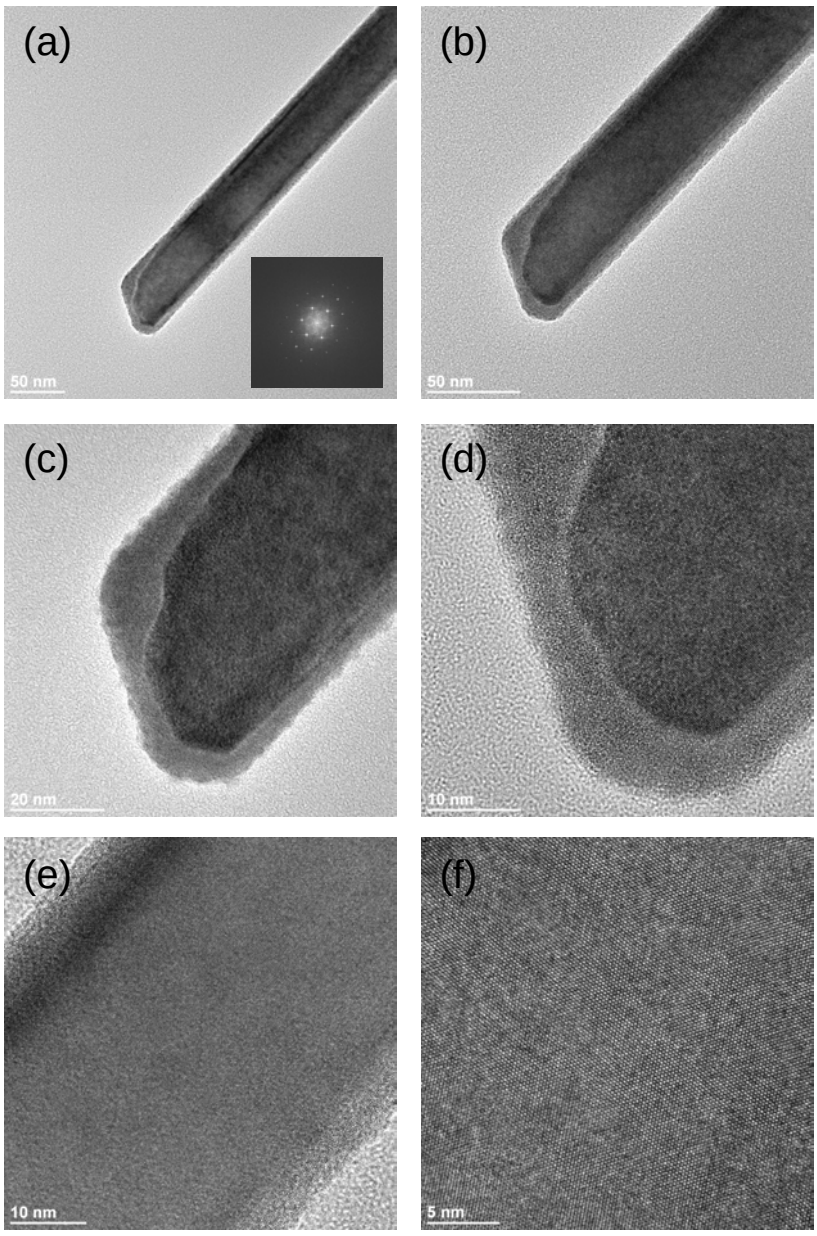


Figure 5.14 – *High Resolution TEM images of a $Bi_{1-x}Sb_x$ nanowire. The magnification is increased from top to bottom. (a and b) show the wire morphology. (c and d) are focused at one end of the wire. (e and f) in the center.*

Finally, an EDX analysis was carried out in a JEOL ARM200F TEM in order to measure the Sb composition and its distribution for both a nanowire and a nanoribbon. The figures 5.15 and 5.16 present both the EDX mapping and the EDX profile of the same $Bi_{1-x}Sb_x$ nanowire (corresponding to figure 5.12). In this wire, the Bi and Sb compositions were found to be 80% and 20%, respectively and the alloy seems to be homogeneous in composition. Similarly, the composition and EDX mapping of a nanoribbon are presented in figure 5.17. The mean Bi and Sb compositions for this ribbon are 67% and 33% respectively, however, an increase of the Sb composition is present at both ends. This could be the signature a VLS growth mechanism, where Sb could be the catalyst.

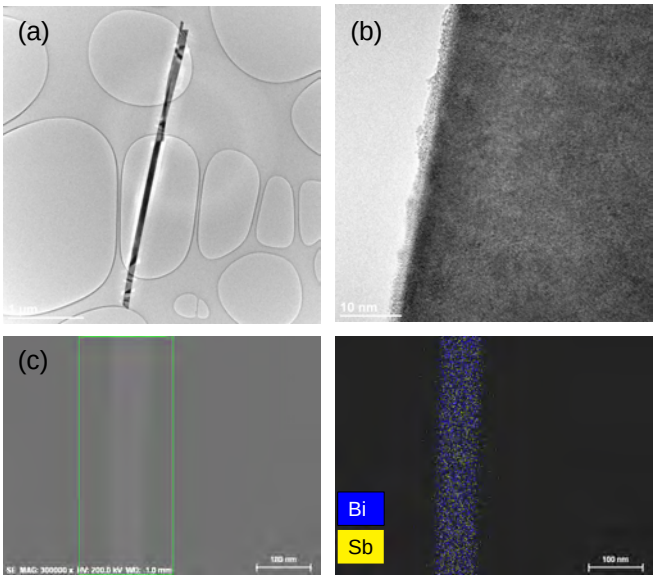


Figure 5.15 – *EDX mapping of a $Bi_{1-x}Sb_x$ nanowire. (a) low magnification TEM image showing the shape of the wire from figure 5.11(b), (b) high-resolution TEM image focused on the edge, (c) region where the EDX measument is carried out and (d) EDX mapping of the nanowire (Bi in blue, Sb in yellow) .*

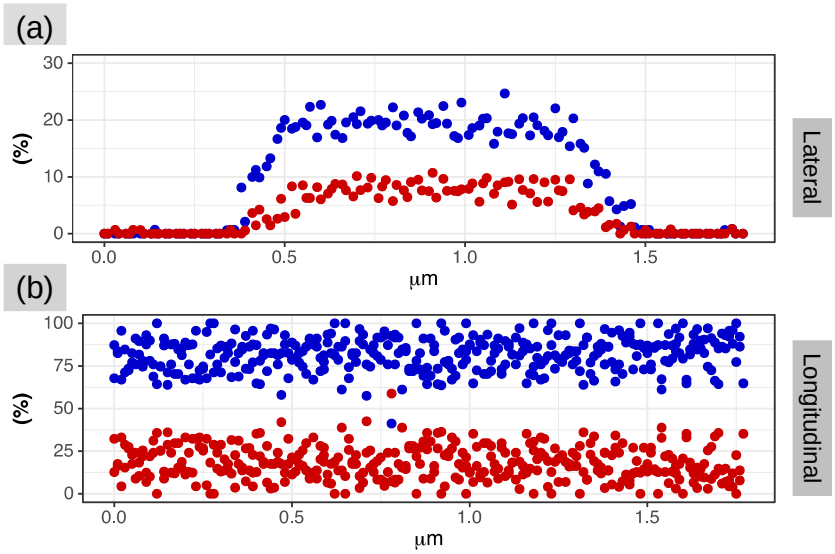


Figure 5.16 – *EXD profiles of a $Bi_{1-x}Sb_x$ nanowire.(a) in the lateral direction and (b) in the longitudinal direction*

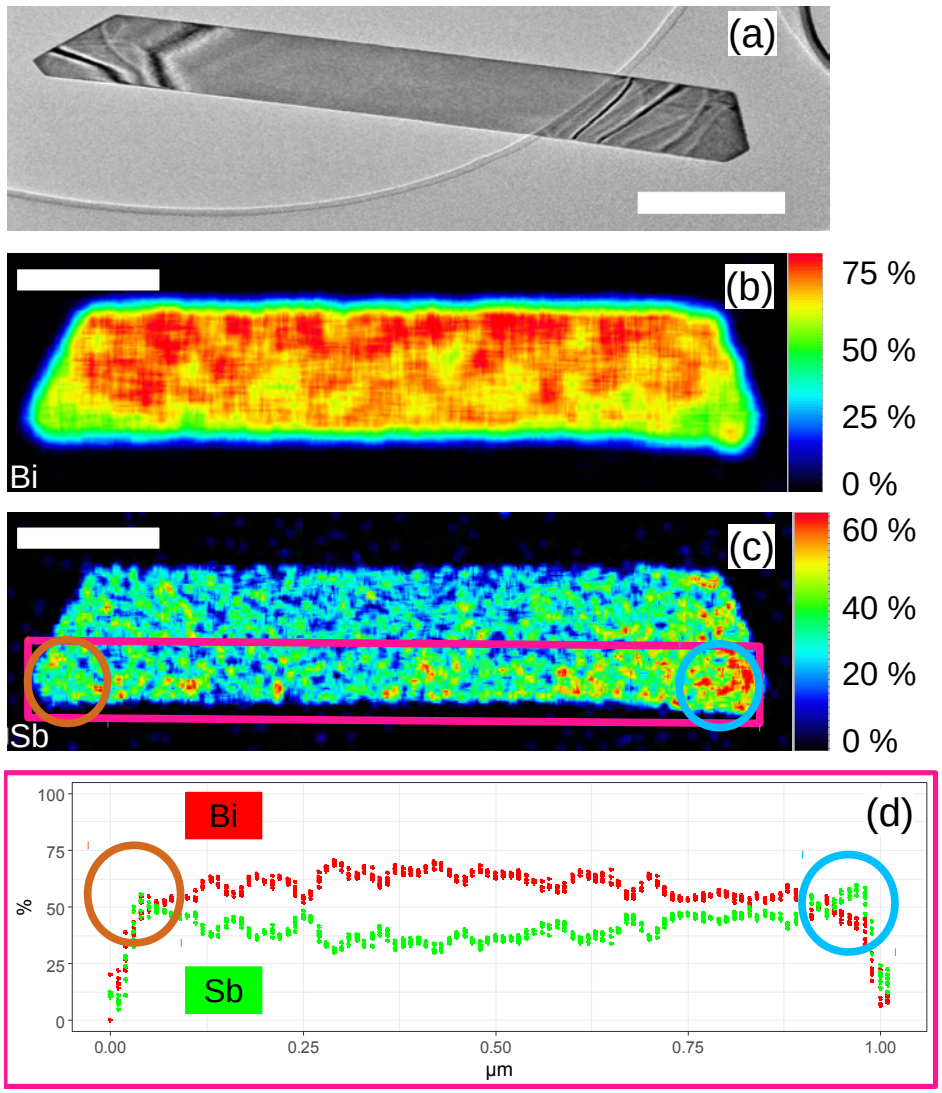


Figure 5.17 – *EDX mapping of a $Bi_{1-x}Sb_x$ nanoflake from figure. 5.11 (a) low resolution TEM image of the flake, (b) Bi compositional mapping of the flake, (c) Sb compositional mapping of the flake and (d) EDX mapping of the pink region of (c) with Bi in Red and Sb in Green. The two circles in (c) and (d); (brown in left and cyan in right) in (d) correspond to an increase of the Sb composition. Scale bars are 250nm.*

After these first growth series, results can be summarized as:

(i) three kind of nanostructures are present: (a) nanowires, (b) nanoribbons and (c) nanoflakes.

(ii) the growth direction is [11-20] in the hexagonal coordinate system.

(iii) the crystalline structure is rhombohedral, defect-free and single crystalline.

These results are particularly promising, but the Sb composition of the alloy is still too high to get a Topological Insulator behavior.

In the following section, our investigations will be focused on controlling the Sb composition changing three growth parameters: (i) the Bi flux , (ii) the Sb flux and (iii) the growth temperature.

5.6.2 Control of Sb compostion in $Bi_{1-x}Sb_x$ nanostructures

As presented in figure 5.9, the antimony composition in $Bi_{1-x}Sb_x$ nanostructures should be in the range 7-22 % for having a 3D Topological Insulator. In order to control the Sb composition, the density of nanostructures and their shape, a complete growth study was performed based on different Bi and Sb fluxes and growth temperatures as presented in figure 5.18. This 3D growth matrix is based on 27 samples, which should be sufficient to understand the observed trends. Finally, since a growth time of one hour leads to the growth of 20 µm long wires, it was decreased to 20 minutes for building up this matrix.

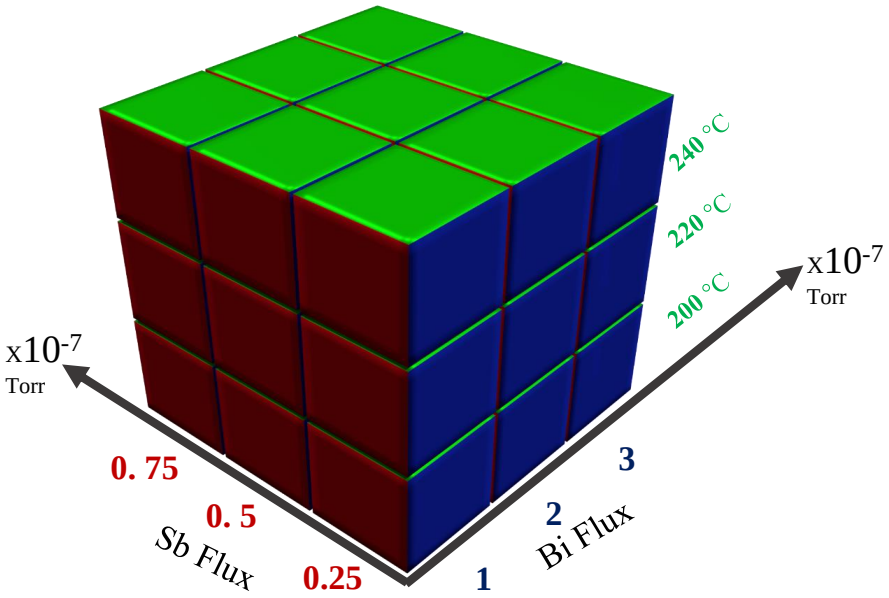


Figure 5.18 – *3D matrix of the growth parameters for $Bi_{1-x}Sb_x$ nanostructures.*

After a standard HF5% oxide removal (see chapter 4), the Si(001) wafers are immediately loaded into the MBE-412 system and degassed at 300°C for 1 hour. Next, they are transferred into the growth chamber and the sample temperature is raised to the growth temperature. The growth parameters used for this study are: the Bi fluxes are 1, 2 and $3x10^{-7}$ Torr, the Sb fluxes are 0.25, 0.5 and $0.75x10^{-7}$ Torr, and the growth temperatures are 200, 220 and 240°C, respectively. The $Bi_{1-x}Sb_x$ alloys are grown by opening the Bi and Sb shutters at the same time. The growth ends by closing both shutters after 20 minutes. Samples are cooled down to 100 °C in the growth chamber before being unloaded and characterized in the SEM (Aztec-600i).

The three figures 5.19, 5.20 and 5.21 present SEM images of the 27 samples. Each figure corresponds to a slice of the 3D growth cube for a fixed temperature: 240, 220 and 200°C respectively. The Bi flux increases from left to right and Sb one from top to bottom. Interestingly, in the three cases, higher Bi and Sb fluxes favor the nanostructure growth and density. Moreover, if the growth temperature is decreased, the nucleation of nanostructures for low Bi and Sb fluxes is favored; even if more 2D parasitic growth can also be observed. In particular, if we consider a Bi flux of $3x10^{-7}$ Torr and a Sb one of $0.5x10^{-7}$ Torr, nanostructures can only be observed at low temperature (i.e.

200°C). This can be interpreted as a higher evaporation rate of bismuth materials at these temperatures compared to antimony. Overall, this suggests that a low growth temperature is needed in order to grow Topological Insulator $Bi_{1-x}Sb_x$ alloys, which also favors 2D bulk growth (leading to a lower density of nanostructures). Finally, almost no nanostructures are observed when the Sb flux is too low ($0.25x10^{-7}$Torr) independently of the Bi flux and the growth temperature. Taking into consideration the observations of section 5.6.1, this could further confirms that a Sb droplet is needed for nucleation and growth.

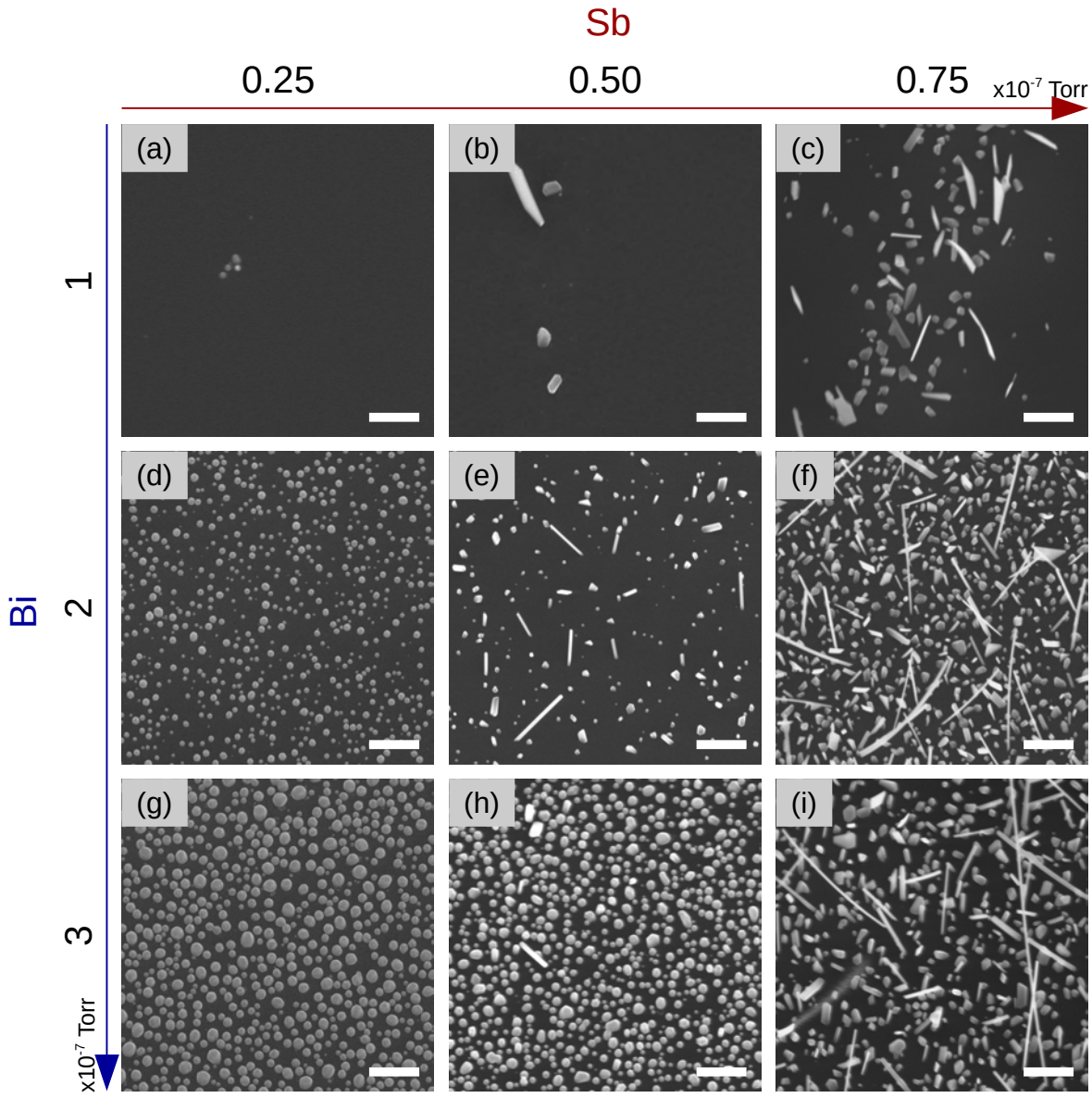


Figure 5.19 – *Slice of the 3D $Bi_{1-x}Sb_x$ growth matrix corresponding to 240 °C on Si(001). The bismuth flux increases from top to the bottom and the antimony flux from left to the right. Each SEM image represents the sample surface for each set of growth parameters. The growth time is 20 minutes. Scale bars are 500 nm.*

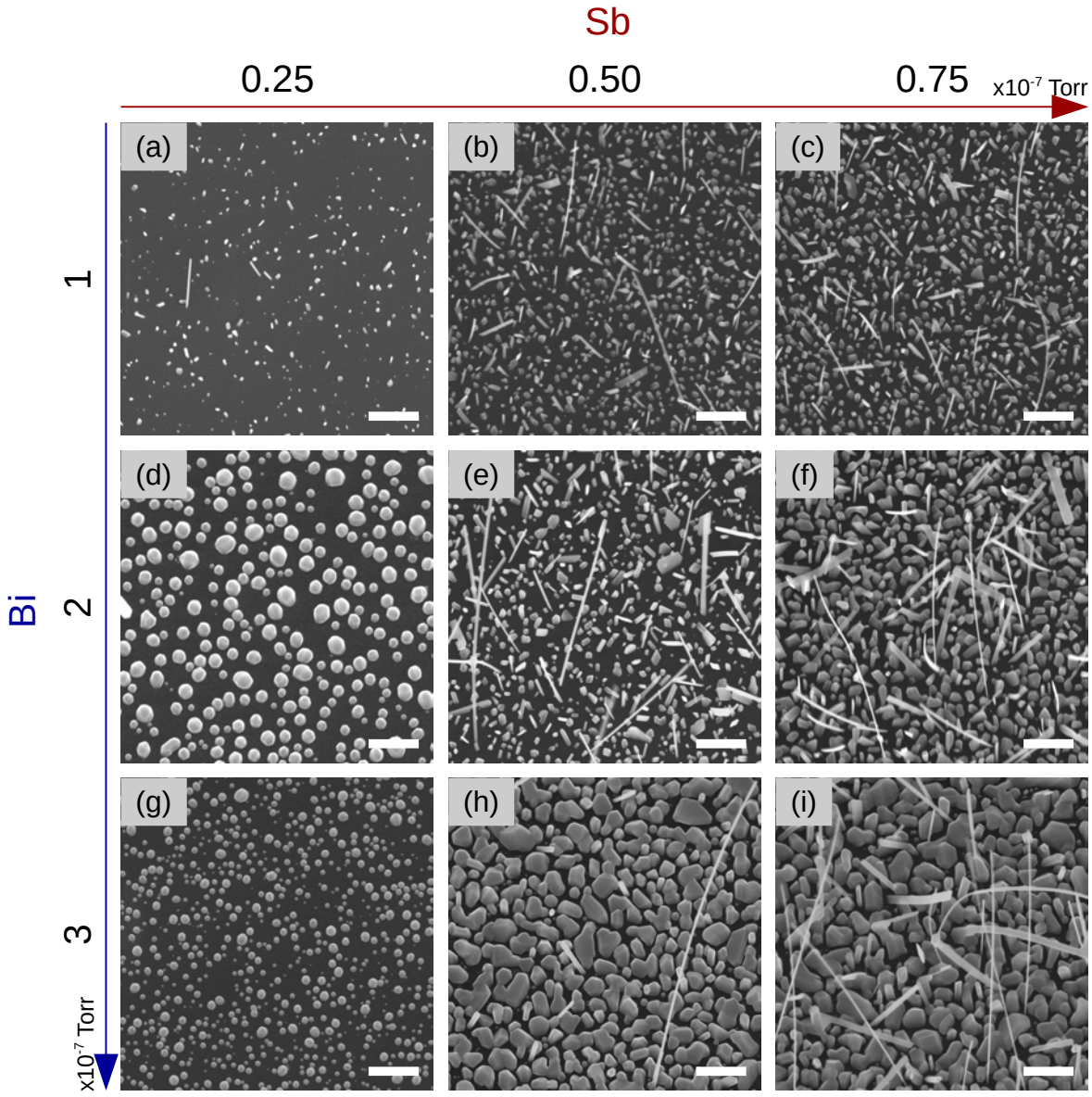


Figure 5.20 – *Slice of the 3D $Bi_{1-x}Sb_x$ growth matrix corresponding to 220 °C on Si(001). The bismuth flux increases from top to the bottom and the antimony flux from left to the right. Each SEM image represents the sample surface for each set of growth parameters. The growth time is 20 minutes. Scale bars are 500 nm.*

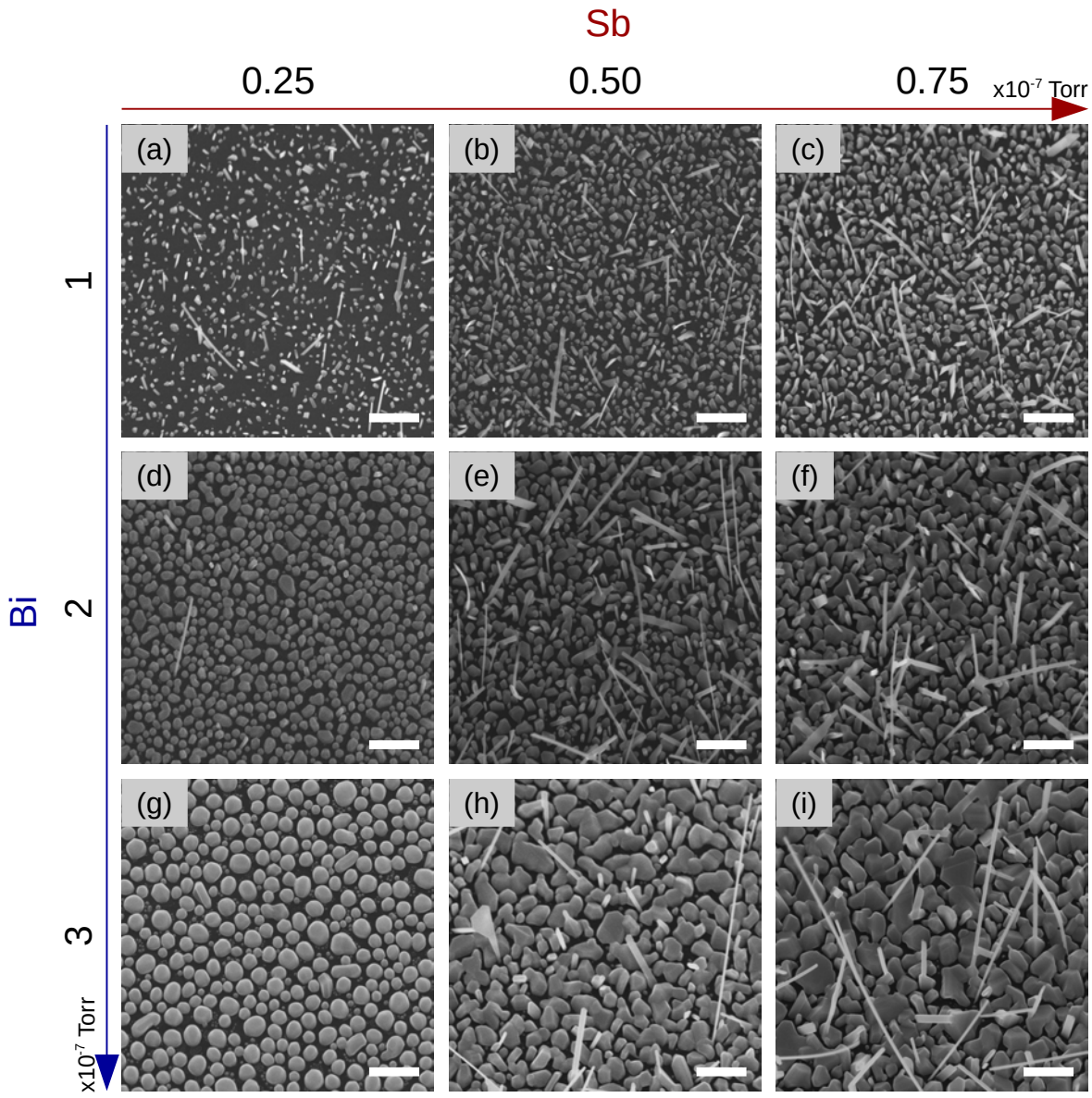


Figure 5.21 – *Slice of the 3D $Bi_{1-x}Sb_x$ growth matrix corresponding to 200 °C on Si(001). The bismuth flux increases from top to the bottom and the antimony flux from left to the right. Each SEM image represents the sample surface for each set of growth parameters. The growth time is 20 minutes. Scale bars are 500 nm.*

5.6.3 XRD of Growth Matrix

In order to measure the Sb composition (x) in $Bi_{1-x}Sb_x$ alloys at the macroscopic level, XRD powder diffraction patterns were recorded for each sample. The advantages of this method, compared to EDS measurements in a TEM, are to give an average composition of the sample and a fast feedback, which allows to adjust the growth parameters. Basics of the XRD instrumentation are presented in chapter 2. In this section, we present the powder diffraction measurement together with the analysis method allowing to compositional determination. Finally, the calculated XRD compositions are presented and the epitaxial parameters influence is discussed.

5.6.3.1 The Powder Diffraction measurement

The X-Ray powder diffraction is one of the most widely used technique to study polycrystalline materials. The working principle is based on the Bragg's law, which was discussed in chapter 2. The powder diffraction spectrum obtained from this technique gives a series of peaks that corresponds to different d-spacing in the $Bi_{1-x}Sb_x$ alloy. The peak position and intensity, as shown in figure 5.22, can be used to identify the corresponding diffracting planes, which can inform on the material crystalline structure and composition. Since the $Bi_{1-x}Sb_x$ nanostructures have no direct epitaxial relationship with the substrate and are randomly oriented, the XRD measurements can either be a classical (ϑ-2ϑ) or a Grazing Incidence XRD (GIXRD) one. Contrary to the (ϑ-2ϑ) measurement presented in chapter 2, the GIXRD uses small incident angles for the incoming X-Ray, so that diffraction can be made surface sensitive, which is favorable for measuring nanostructures. Indeed, the wave penetration is limited, so that only the surface contributes to the diffraction pattern.

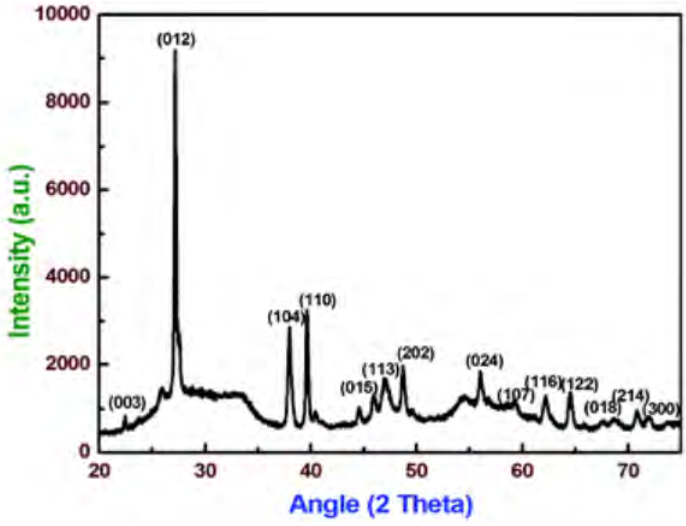


Figure 5.22 – *Representative X-ray diffraction patterns of ultrathin Bismuth nanosheets.. The peaks match well with powder X-ray diffraction pattern for rhombohedral phased bismuth with cell parameters a = 4.545 Å and c = 11.83 Å. (Kumer et al.[323])*

5.6.3.2 The XRD Results

First the 27 samples presented in the 3D growth matrix figure 5.19, 5.20 and 5.21 were measured by GIXRD, and the corresponding powder diffraction patterns are reported in figure 5.23. In this figure, the Sb flux varies from left to right, the Bi from top to bottom and the three different colors represent the growth temperatures. Following the XRD measurements, each sample data is analyzed and an XRD composition is consequently attributed to them. The following subsection details the analysis part of these raw XRD measurements.

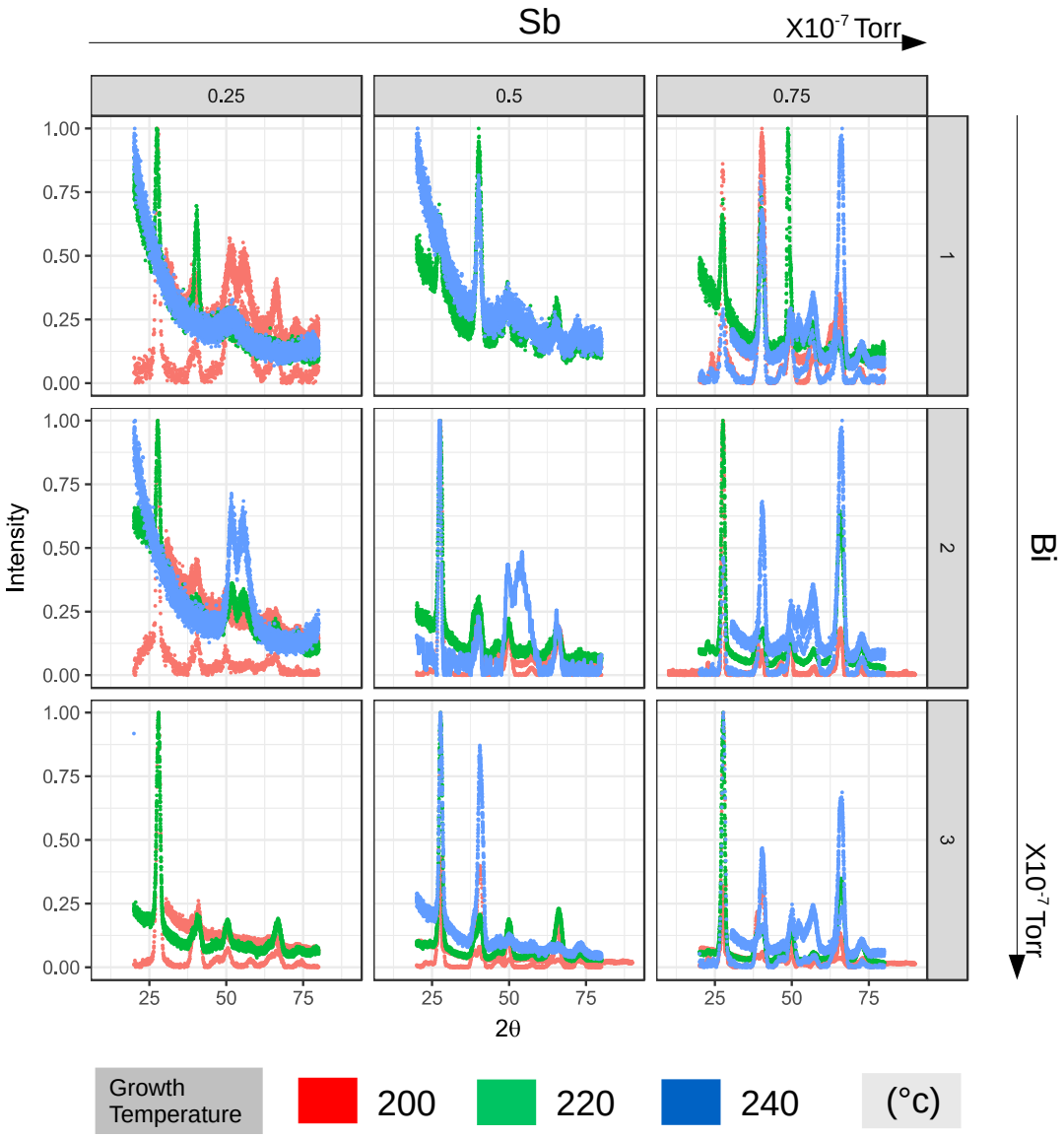


Figure 5.23 – *Recorded XRD of all samples belonging to different temperature planes as shown in figure 5.19, 5.20 and 5.21. Each subplot presents 3 unique (whenever possible) recorded raw XRD measurements with 2ϑ on the x-axis and the normalized XRD peaks on y-axis. Bi flux increases from top to bottom and Sb from left to right. Different colors corresponds to different growth temperature.*

5.6.3.3 Analysis of the XRD measurements

In the Bragg's equation, if only one reflection is considered (n=1), the d-spacing can be estimated as $d = \frac{\lambda}{2sin\theta}$, where λ is the wavelength of the X-ray source (1.54059 Å), and θ is given by the experimental diffraction spectrum. Since the lattice parameter of the $Bi_{1-x}Sb_x$ crystal depends directly of its antimony composition, the diffracting spectrum, i.e. the angle and intensity of the diffracted peaks, are directly correlated to the Sb composition. Due to the $Bi_{1-x}Sb_x$ crystalline symmetry, the intensities of the diffracting [h,k,l] planes are not equal. In order to determine the brighter ones, a VESTA[324] modeling of the crystalline structure was developed, leading to only consider the following [h,k,l] planes: [003], [10-2], [104], [2-10], [2-13], [202], [3-1-2]. In parallel, the intensity and the 2θ angle of the 4 to 6 brightest peaks were measured, using Peak Fit 4.0[325] and a Gaussian peak distribution. Next, a [h,k,l] plane was attributed to each of these peaks, depending of 2θ (Note here that correlating 2θ to the intensity allows to avoid mistakes).

Once a [h,k,l] plane is attributed to each measured peak, it is possible to compare the 2θ measured angle to the theoretical one. Indeed, Dismukes et al.[318] (see figure 5.24) measured the lattice parameters of the $Bi_{1-x}Sb_x$ alloys as a function of the Sb composition and Jain et al.[326] proposed an equation to calculate the d-spacing in $Bi_{1-x}Sb_x$ (see the following equation 5.1).

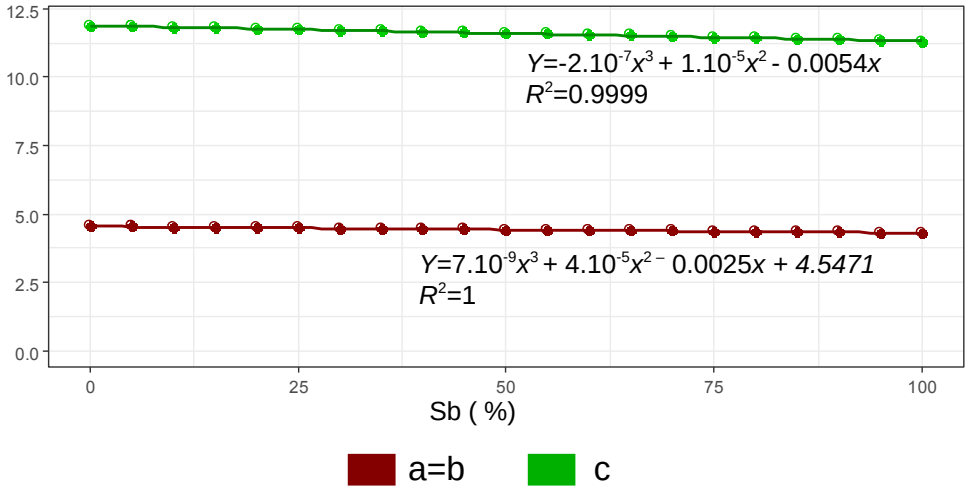


Figure 5.24 – *Lattice parameters with respect to Sb reference*

$$\frac{1}{d_{hkl}^2} = \frac{4}{3}\frac{h^2+hk+k^2}{a^2} + \left(\frac{l}{c}\right)^2 \tag{5.1}$$

Using a 3rd order polynomial fit of Dismukes' values (see figure 5.24), it is then possible to calculate the $Bi_{1-x}Sb_x$ lattice parameters (a, b and c) as a function of the Sb composition and thus to calculate the d-spacing for each composition and plan. Then, using the Bragg's equation, it is possible to calculate a theoretical diffracting 2θ angle corresponding to a family of plans and to a composition.

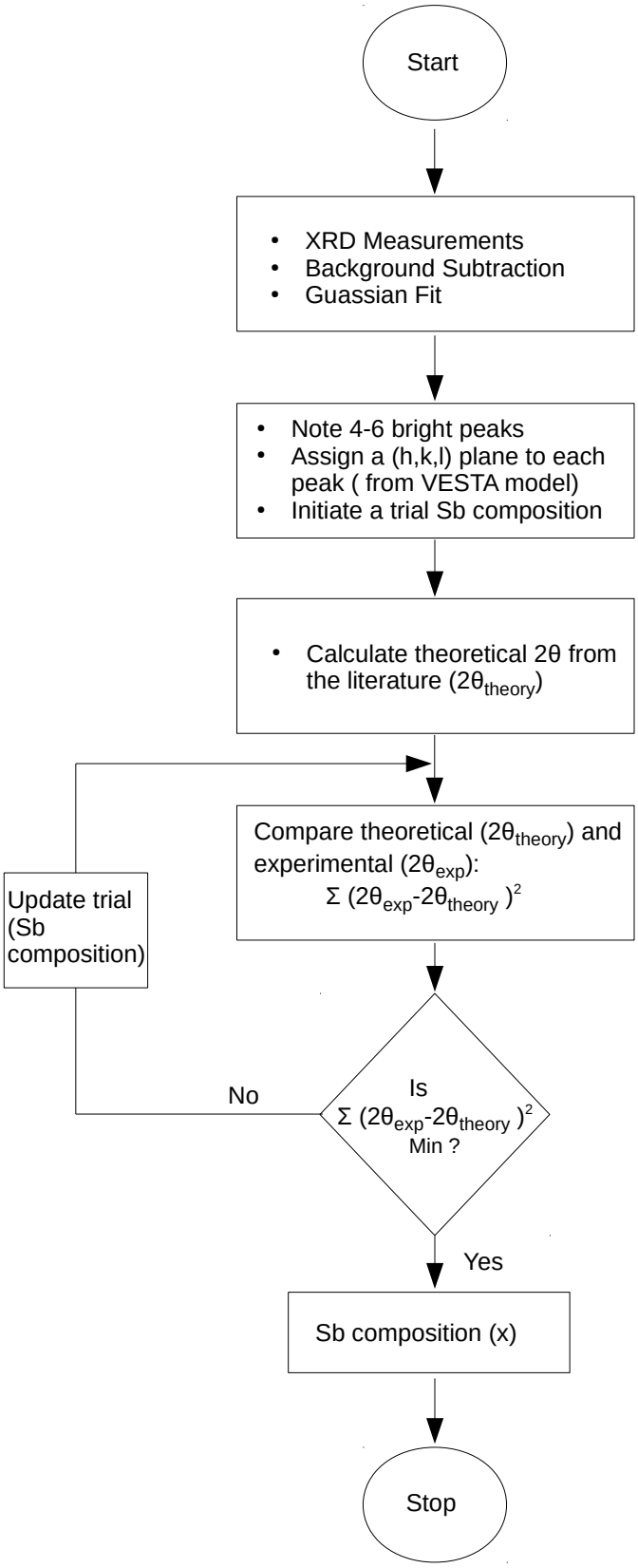


Figure 5.25 – *Flowchart for XRD peak analysis*

By comparing these theoretical and measured 2θ angles, it is finally possible to build an "error" function for each [h,k,l] plane, minimize it as described in the figure 5.25 and get a macroscopic Sb composition for each sample.

The figure 5.26 reports the macroscopic Sb composition of $Bi_{1-x}Sb_x$alloys. In this figure, the growth temperature increases from left to right and for each subplot, the x-axis corresponds to the Bi flux and the y-axis represents the measured Sb composition. Interestingly, the Sb compostion of few samples is in the 3D TI range (region between lower and upper brown line), which proves the possibility to grow and control these new $Bi_{1-x}Sb_x$ nanostructures. Moreover, it also highlights the need to optimize the three growth parameters. It can also be noticed that a low growth temperature with a high Bi and a low Sb flux is needed to reach the 3DTI region.

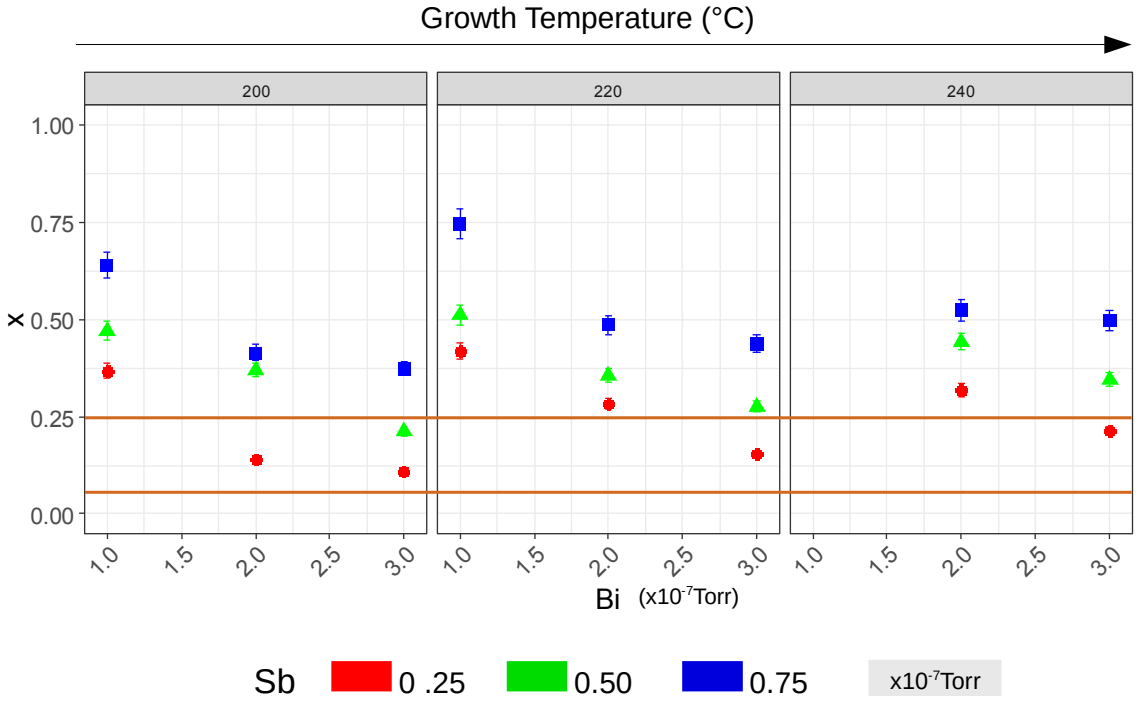


Figure 5.26 – *Sb composition of $Bi_{1-x}Sb_x$alloys measured by XRD for each sample. The growth temperature increases from left to right. The x-axis corresponds to the Bi flux, the y-axis is the measured XRD composition. The different Sb fluxes are represented by different colors. Two horizontal lines (in brown) indicate the lower (7%) and upper (25%) limits of composition for $Bi_{1-x}Sb_x$ to behave as a 3D TI.*

Interestingly, the measured XRD compositions are not directly equals to the flux ratios ($Sb/(Bi+Sb)$), but a temperature dependent linear fit $y = ax + b$ can be calculated, where y is the resulting XRD composition, x is the flux ratio ($Sb/(Bi+Sb)$) and a and b are two temperature dependent parameters. The a and b values are reported in the table 5.2. Interestingly, this further confirms the higher evaporation rate of Bismuth compared to Antimony in this range of temperature (200-240°C) contrary to what is reported in literature[318,326].

Growth Temperature (°C)	Equation	a	b	Error $(\sum(\varphi' - \varphi)^2)$
200	y=1.463x+0.024	1.463	0.024	0.0014
220	y=1.516x+0.077	1.516	0.077	0.0147
240	y=1.615x+0.038	1.615	0.038	0.8816

Table 5.2 – *Linear equation on the basis of different temperature*

Finally, a macroscopic and microscopic comparison of the measured compositions is reported in table 5.3, where the XRD and the EDS-TEM compositions are reported for the same samples. Both values are in good agreement proving that macroscopic and microscopic behavior are the same. This further confirms that XRD measurements are predicting very accurately the nanostructure compositions.

Bi Flux (x10^{-7} Torr)	Sb Flux (x10^{-7} Torr)	Growth Time (minutes)	Sb composition (%) (TEM-EDS)	Sb composition (%) (XRD)
1	0.25	60	26	28
1	0.50	60	19	25
1	0.75	60	53	55
3	0.50	20	20	23

Table 5.3 – *Comparison of the XRD and EDS-TEM composition of $Bi_{1-x}Sb_x$ nanostructures.*

5.6.4 Advanced characterizations

Finally, in order to determine the nanowires facets, a cross-sectional TEM characterization was carried out as shown in figure 5.27. First, the $Bi_{1-x}Sb_x$ nanostructures were mechanically transferred onto the SiO_2 substrate [figure 5.27 (a)]. From the SiO_2 substrate, a region was chosen for the FIB cut [Red inset in figure 5.27 (a)]. Following a carbon and palladium deposition was performed and the nanowire was cut [figure 5.27 (b and c)]. Figure 5.27 (d) and (e) present the nanowire facets and the compositional heatmap. 3 pairs of facets are clearly visible: the <0001>, <1101> and <1102> families in the hexagonal coordinate system, which corresponds to the <001>, <111> and <112> families in the cubic one. From 5.27(d and e), we can also consider that facets are not equal in length: as <1102> facets are considerably shorter. In figure 5.27(d), the heatmap was constructed with Bi in red and Sb in green. Interestingly, the Bi and Sb distribution is not uniform in the cross-section. In figure 5.27(f), a 2D modeling of the cross-section was developed with VESTA. The compositional heterogeneity depends directly of the facet nature: the <1101> family is Bi rich (~10% compared to the sample mean) whereas the <0001> is Sb rich. This could lead to different 3D TI behavior on these facets, which will be studied later in the ANR:HYBRID project.

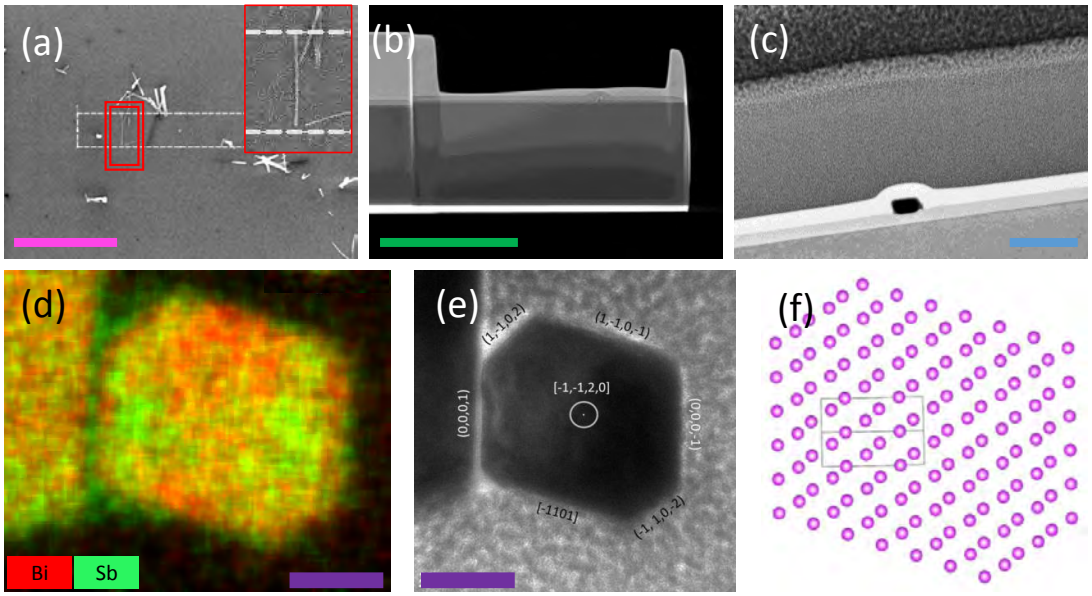


Figure 5.27 – *Cross-sectional characterizations of a $Bi_{1-x}Sb_x$ nanowire. (a) The original SEM image of the transferred nanostructures on SiO_2 substrate. The red inset shows the region that was chosen for FIB cut. (b) The image after the FIB cut once carbon and palladium are deposited. (c) Low resolution TEM image of the FIB cut. (d) (EDS) measurement of the cross-section. (e) Determination of the nanowire facets. (i) VESTA modeling of the cross-section. Scale bars are: 500 nm for (a),(b) and (c) ; 20 nm for (g) and (h).*

5.7 Conclusions and outlooks

In conclusion, $Bi_{1-x}Sb_x$ nanostructures, which includes nanowires, nanoflakes and nanoribbons, are successfully integrated on Silicon by MBE for the first time. Remarkably, these nanostructures are defect free and the growth direction is (110) in the cubic system. A 3D growth matrix was developed in order to assess and understand the influence of the growth parameters including the bismuth and antimony fluxes and the growth temperature. Interestingly, the macroscopic and microscopy chemical analyses are in good agreement and $Bi_{1-x}Sb_x$ nanostructure composition is in the Topological Insulator range.

In addition, we noticed that a minimum Sb content is mandatory for the nucleation of $Bi_{1-x}Sb_x$ nanostructures, whatever the growth temperature is. More importantly, we report from the TEM-EDS characterization of a nanoflake, that the Sb composition was higher at one end of the flake. These two informations strongly hints towards a Sb mediated VLS growth mode.

Furthermore, no material was deposited at higher temperature and bulk growth started to become prominent below 200 °C, particularly when the Bi flux is high. This could mean a higher evaporation rate of Bi compared to Sb, however it is too early to make any conclusions. A study focusing on the nucleation and growth mechanisms should unveil further informations on this and we suggest also since long growth time (60 minutes at 235 °C) can lead to the growth of high density nanostructures, whereas 20 minutes growth gave almost nothing. This indirectly suggests that an accumulation of material is maybe needed for nucleation.

Similarly, the higher Bi content on <1-101> facets is also particularly interesting considering that the first 3D TI behaviour was confirmed on this surface. The higher Bi content on this surface, means that it should be possible to get a TI surface without necessarily getting a bulk 3D TI.

However, additional characterizations are still needed to confirm the nanoscale topological insulator behavior of $Bi_{1-x}Sb_x$ nanostructures including STM measurements in order to assess the electronic surface states; and NanoARPES characterizations to probe the topological insulator behavior. It is worth to mention that these characterizations are in progress, as well as the development of new nanoscale $Bi_{1-x}Sb_x$ TIs as part of the Hybrid ANR-PIRE project. Additional information are available here: http://www.agence-nationale-recherche.fr/Projet-ANR-17-PIRE-0001.

Finally, a growth on a deoxydized Si(110) wafer was carried out with Bi and Sb flux of $3.0x10^{-7}$ and $0.5x10^{-7}$ Torr respectively for 20 minutes at the growth temperature of 205 °C. Figure 5.28 presents a SEM image of this growth and it is noticable that the nanowires are growing in different directions including the vertical one as shown in the red inset. Hence, it should be possible to integrate $Bi_{1-x}Sb_x$ nanowires vertically on patterned and Si(110) substrates. On the other hand, the epitaxial integration of a superconductor, such as Al or V, on these structures could lead to better topological Qubits. Likewise, from the material engineering side, MBE growth of other 3DTIs would be also interesting including: Bi_2Se_3, Bi_2Te_3, $Bi_2Te_2Se_1$[BTS 221] and $(Bi_{1-x}Sb_x)_2Te_3$.

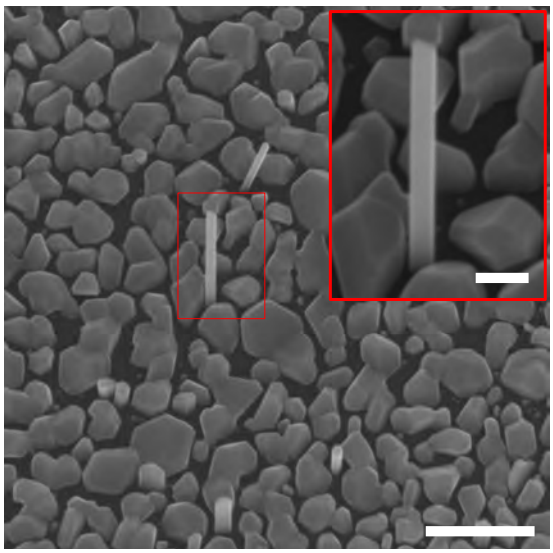


Figure 5.28 – *$Bi_{1-x}Sb_x$ nanostructures on Si(110). Scale bars are: 500 nm for the big image and 100 nm for the red inset.*

General Conclusion

This thesis focuses on the bottom-up integration of InAs and $Bi_{1-x}Sb_x$ nanowires on Si for nanoelectronics and topological Qubits by Molecular Beam Epitaxy (MBE). Nanowires are 1D nanostructures with diameter in 10's of nanometers and length in few microns. The general interests of this geometry is summarized for 10 possible applications that are briefly presented in the first chapter of the thesis. On the other hand, chapter 2 and 3 focus on the description of tools used during the thesis and present the general theory behind nanowire growth.

Next, in chapter 4 we present our contribution for addressing few bottlenecks of InAs nanowires integration on silicon. The full CMOS standards strictly demands fully vertical thin and long self-catalyzed nanowires on Si without crossing the thermal budget of 450 °C. Fully vertical and self-catalyzed InAs nanowires on Si were demonstrated 10 years ago by a group from Japan for a Metal Oxide Vapor Phase Epitaxy (MOVPE) system. Since then, other MOVPE groups were able to match these results, whereas the MBE groups faced significant difficulties. In this thesis, considering the H_2 environment as the main difference, we integrated an in-situ H_2 preparation in our MBE system. The first two growths confirmed the key role of H_2 . Following, we demonstrated very high yield (~90%) of InAs and InAsSb on patterned Si wafers. Next, we developed a process invovlving either H_2 gas or H_2 plasma in order to avoid crossing the Back-End-of-Line (BEOL) thermal budget. A full growth analysis was carried out for both the gas and plasma treatments, which prove the different surface termination obtain in both case. We even revealed a Vapor-Solid (VS) to Vapor-Solid-Liquid (VLS) change in the growth mode thanks to statistics.

On the other hand, $Bi_{1-x}Sb_x$ alloy was the first confirmed as a 3D Topological Insulator (TI). 3D TIs are new phase of matter which conduct on the suface but have an insulating bulk. These robust surface states can be engineered to host Majorana fermions that can be used as Qubits. Compared to the existing 1D semiconducting nanowires based topological qubits, a 1D 3DTI is supposed to be beneficial for industrialization. In chapter 5, we start the growth of this new material from the scratch and in no time manage the first $Bi_{1-x}Sb_x$nanostructures (nanowires, nanoribbons and nanoflakes). The TEM characterizations reveal that these nanowires are defect free and the growth direction is (110). Similarly, in order to control the Sb composition in the alloy and understand the influence of the growth parameters (the Bi flux, the Sb flux and the growth temperature), a full study of 27 samples was carried out. The Sb composition was controlled between 15% and 50% both at nanoscale and macroscopic level. Finally, cross-sectional TEM and EDS characterizations revealed the faceting of these nanostructures and a segregation effect depending of the facet nature.

In the case of InAs, perspectives are the optimization of the CMOS compatible process for growth in patterns. It will be also interesting to increase the Sb content in InAsSb nanowire arrays. In the case of $Bi_{1-x}Sb_x$, the first goal will be to decrease further the Sb composition in order to cover the full TI range (from 4% to 22%). Next will be the growth on Si(110) substrates in order to have vertical integration on silicon (+patterns). Finally, the integration of superconducting materials on nanoscale $Bi_{1-x}Sb_x$TIs could lead to better nanoscale topological Qubits.

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Appendix A

A Hydrogen plasma cell was integrated on the preparation chamber of the Riber MBE-412 reactor. Figures A.1, A.2, A.3 and A.4 illustrate the setup and the step by step procedures for hydrogen preparation surface preparation. The hydrogen gas bottle, in the left, is the source of hydrogen, while the degas chamber, in the right is the destination of this gas or plasma. In order to ignite plasma, a RF cavity is present. Similarly, to control the hydrogen flow, two systems are present: a regulator and a MAF sensor. The whole system is equipped with a pumping system that can reach 10^{-5} Torrs. The plasma cell is cooled down thanks to a water circuit since the surface treatment can generate significant amount of heat.

Figure A.1 shows the basic set-up while the system is not in operation. Once the vacuum level reaches 10^{-5} Torr, all the valves are closed, and the line is pumped by the degassing chamber.

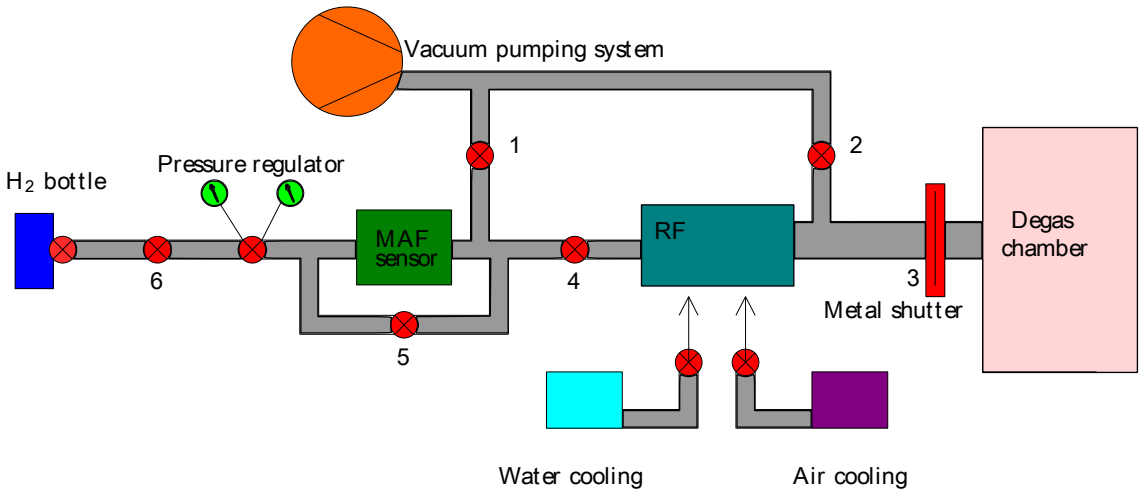

Figure A.1 – *Hydrogen treatment setup.*

Figure A.2 shows the initial pumping stage in order to create a vacuum of at least 10^{-5} Torr before the treatment. In this step, the vaccum is created in the whole line by opening the necessary valves. This process lasts for about 10-15 minutes.

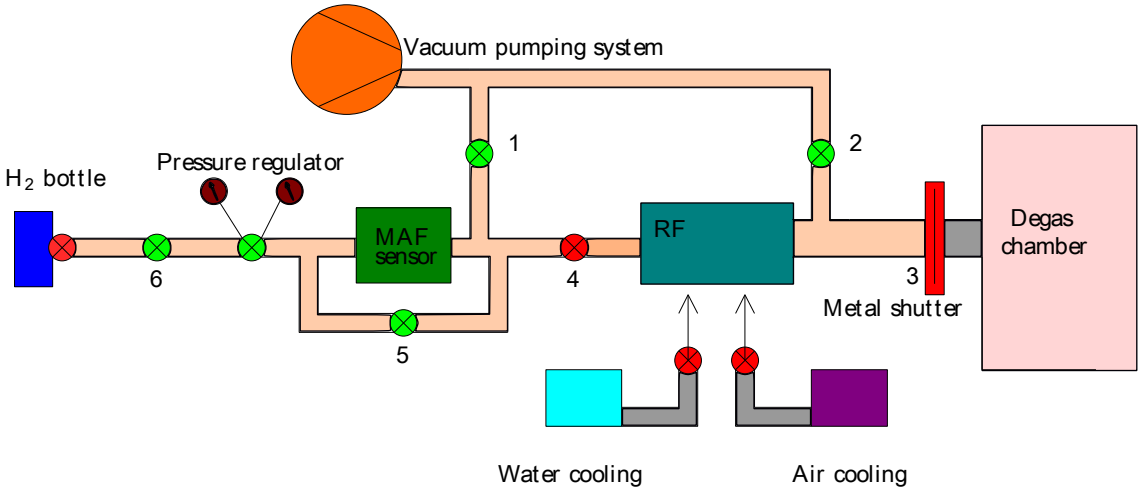

Figure A.2 – *Creating Vaccum in the preparation setup.*

Following the initial pumping, the system is ready for the operation and figure A.3 presents this step. Once the temperature in the degas chamber is adjusted, first the desired amount of hydrogen is collected in the region between the hydrogen bottle and valve 6 by opening the valve of the bottle for a short period. Following, the pressure regulator and MAF sensor are adjusted to get the required amount of hydrogen. The RF cavity ignites the plasma if needed and the surface treatment can be started by opening the shutter between the cell and the degas chamber. The preparation ends by closing the shutter.

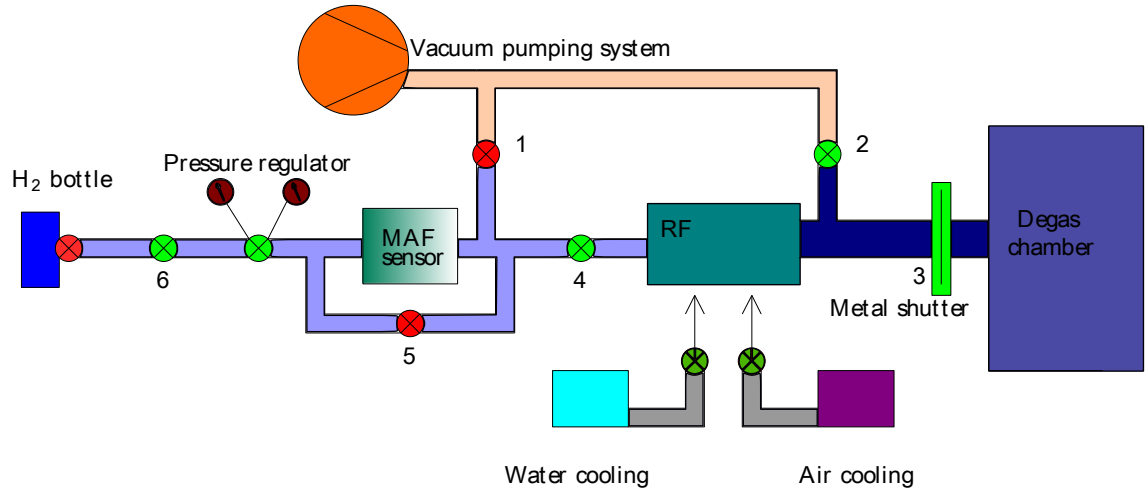

Figure A.3 – *Plasma Preparation*

In the case of a gas treatment, as shown in figure A.4, the same gas goes directly into the degas chamber.

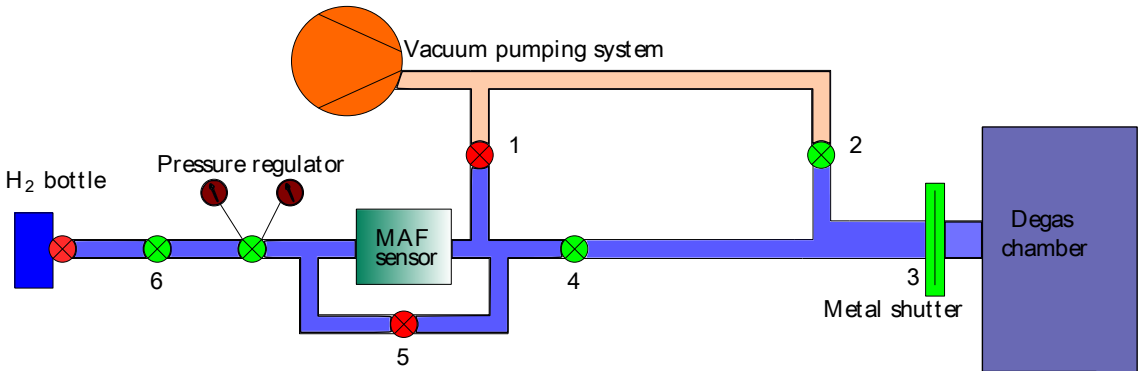

Figure A.4 – *Gas Preparation Setup*

Appendix B

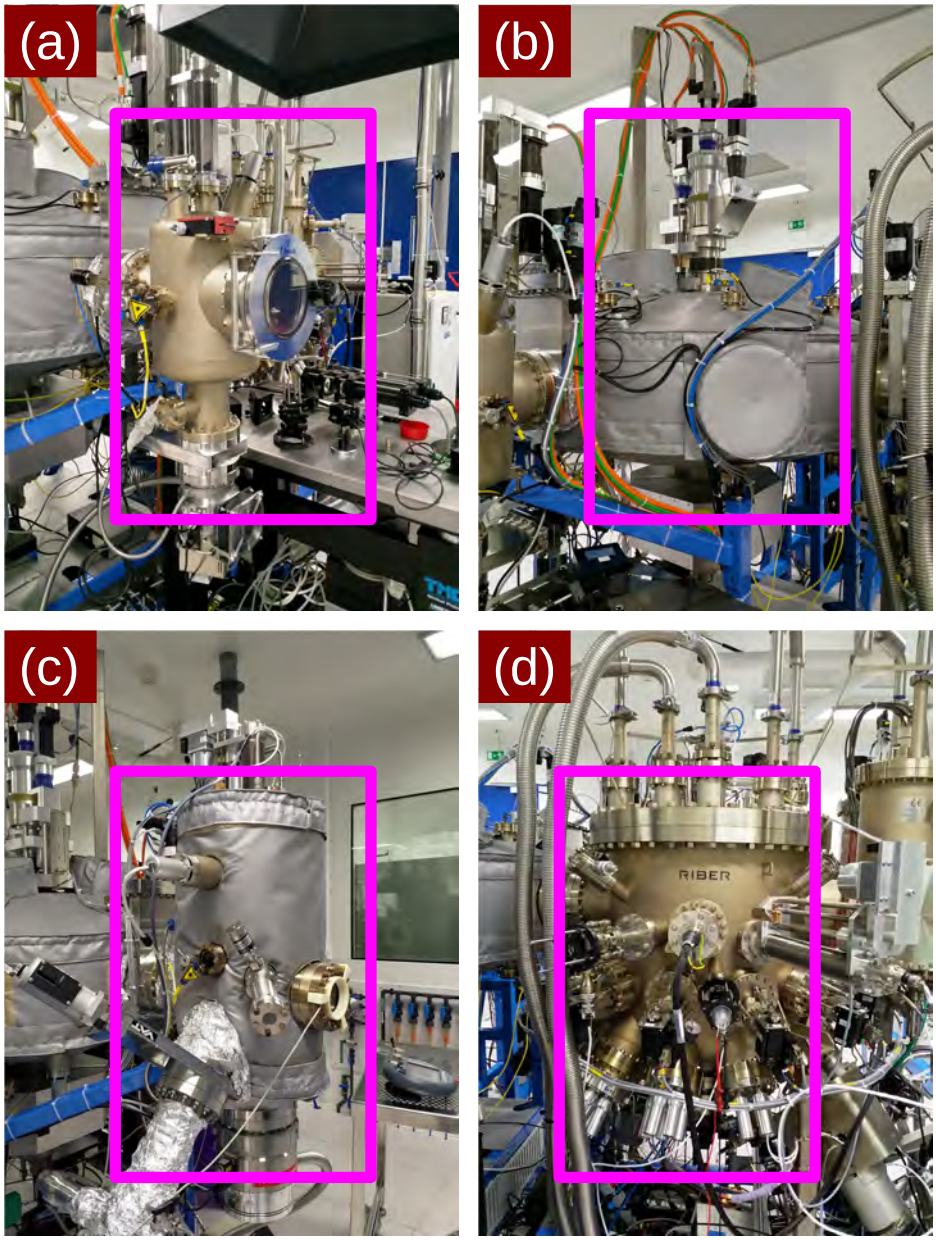

Figure B.1 – *Different parts of the RIBER MBE-412 reactor: (a) the loading chamber, (b) the cluster, (c) the preparation chamber and (d) the growth chamber.*

Appendix C

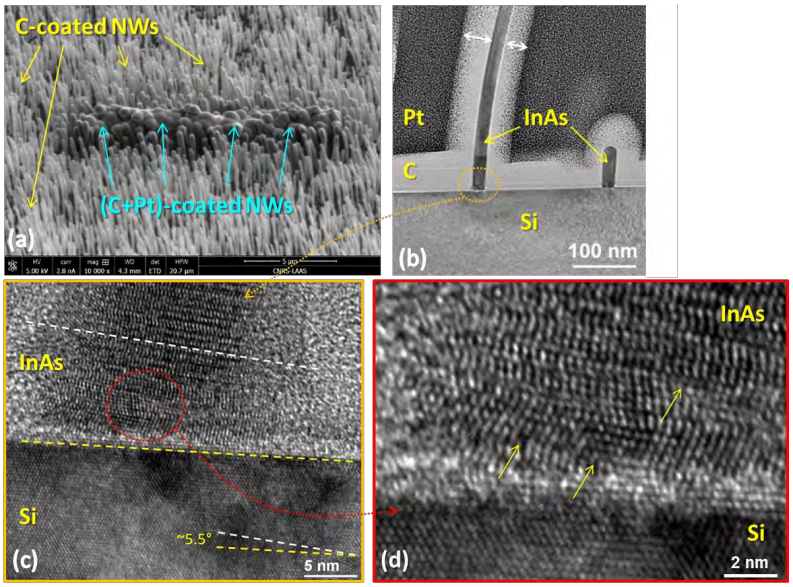

Figure C.1 – *(a) SEM image of InAs nanowires grown on (111)Si substrate taken at the beginning of cross section lamella FIB preparation process. The whole sample is initially coated with Carbon (cf. yellow arrows). Additional Pt deposition is carried out in the area to be thinned by FIB (cf. cyan arrows). (b) Cross-section TEM image of InAs nanowires from FIB prepared lamellas. Non-uniformity in the carbon deposition on each side of the nanowires (cf. white arrows) may result in stress-induced bending of long nanowires (cf. nanowire on the left of the image). (c) HRTEM image of the InAs/Si interface region of the InAs nanowires shown on the left of image (c). In this case, the (111) planes of the InAs nanowire are tilted by ~5.5° with respect to the (111) planes of the Si substrate. (d) Magnified image of the InAs/Si interface region. In this case, induced stress exceeds the plastic deformation threshold and dislocations are formed in the InAs crystal close to the interface.*

Appendix D

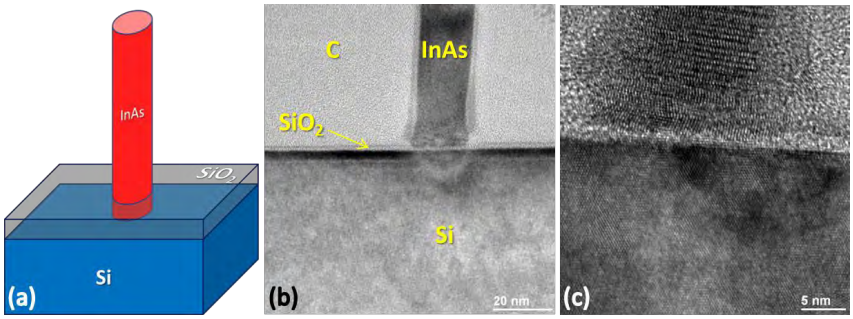

Figure D.1 – *(a) Schematic description of the native SiO_2 layer covering the surface of the Si substrate and surrounding the base of the InAs nanowires. (b) Low magnification conventional bright field TEM image of an InAs nanowire still attached to the Si substrate. The strong contrast originating from the native oxide may suggest that the InAs nanowire is physically separated from the substrate. However, high resolution images taken at higher magnification (c) allow the observation of the crystalline planes throughout the interface, clearly indicating that the InAs growth is epitaxial. An even stronger contrast from the interface region is obtained with STEM/HAADF images, such as those shown in the main text (cf figure. 4.16b, figure 4.16c and figure 4.16d).*

Appendix E

Silicon Oxide Patterning

The procedure used to create patterns on the Silicon wafers is a standard one based on Electron Beam Lithography (EBL):

1. An oxide layer of 20 nm is thermally grown on a brand new Si(111) wafer.

2. The wafer is coated using a spinning rotor with 40 nm of Poly Methyl Methacrylate (PMMA) that is a positive photoresit.

3. The PMMA is impressed using EBL, which moves the beam according to a planned schematic and at a speed that depends on the set electron flux and dose.

4. The PMMA is developed immersing the wafer for 12 s in a pot filled with Methyl Isobutyl Ketone (MIBK). This is the hardest step to reproduce because it is done manually. The sample is then cleaned with Isopropyl Alcohol.

5. The sample is etched with a plasma composed by 50 SCCM of CHF3 and 3 SCCM of O2 which leaves holes and cleaned patches on the silicon oxide according to the zones exposed by the impression-developing steps. The PMMA leftovers are removed using acetone.

6. All the procedure is calibrated so that the opened holes still have a 3 nm oxide at their bottom in order to protect the surface from random and not controlled reoxidation. Thus, before introducing the sample in the MBE chamber, it is etched with a calibrated HF system. In the end the result is a patterned oxide with a thickness of 17 nm and holes perfectly cleaned from any oxide.

Abstract

InAs and $Bi_{1-x}Sb_x$ nanowires with their distinct material properites hold promises for nanoelectronics and quantum computing. While the high electron mobility of InAs is interesting for nanoelectronics applications, the 3D topological insulator behaviour of $Bi_{1-x}Sb_x$ can be used for the realization of Majorana Fermions based qubit devices. In both the cases improving the quality of the nanoscale material is mandatory and is the primary goal of the thesis, where we study CMOS compatible InAs nanowire integration on Silicon and where we develop a new nanoscale topological insulator.

For a full CMOS compatiblity, the growth of InAs on Silicon requires to be self-catalyzed, fully vertical and uniform without crossing the thermal budge of 450 °C. These CMOS standards, combined with the high lattice mismatch of InAs with Silicon, prevented the integration of InAs naowires for nanoelectronics devices. In this thesis, two new surface preparations of the Silicon were studied involving in-situ Hydrogen gas and in-situ Hydrogen plasma treatments and leading to the growth of fully vertical and self-catalyzed InAs nanowires compatible with the CMOS limitations. The different growth mechanisms resulting from these surface preparations are discussed in detail and a switch from Vapor-Solid (VS) to Vapor-Liquid-Solid (VLS) mechanism is reported. Very high aspect ratio InAs nanowires are obtained in VLS condition: upto 50 nm in diameter and 3 microns in length.

On the other hand, $Bi_{1-x}Sb_x$ is the first experimentally confirmed 3D topololgical insulator. In this new material, the presence of robust 2D conducting states, surrounding the 3D insulating bulk can be engineered to host Majorana fermions used as Qubits. However, the compostion of $Bi_{1-x}Sb_x$ should be in the range of 0.08 to 0.24 for the material to behave as a topological insulator. We report growth of defect free and composition controlled $Bi_{1-x}Sb_x$ nanowires on Si for the first time. Different nanoscale morphologies are obtained including nanowires, nanoribbons and nanoflakes. Their diameter can be 20 nm thick for more than 10 microns in length, making them ideal candidates for quantum devices. The key role of the Bi flux, the Sb flux and the growth temperature on the density, the composition and the geometry of nanoscale structures is investigated and discussed in detail.

Résumé en francais

Grâce à leur propriétés uniques, les nanofils d'InAs et de $Bi_{1-x}Sb_x$ sont important pour les domaines de la nanoélectronique et de l'informatique quantique. Alors que la mobilité électronique de l'InAs est intéressante pour les nanoélectroniques; l'aspect isolant topologique du $Bi_{1-x}Sb_x$ peut être utilisé pour la réalisation de Qubits basés sur les fermions de Majorana. Dans les deux cas, l'amélioration de la qualité du matériau est obligatoire et ceci est l'objectif principal cette thèse où nous étudions l'intégration des nanofils InAs sur silicium (compatibles CMOS) et où nous développons un nouvel isolant topologique nanométrique: le $Bi_{1-x}Sb_x$.

Pour une compatibilité CMOS complète, la croissance d'InAs sur Silicium nécessite d'être auto-catalysée, entièrement verticale et uniforme sans dépasser la limite thermique de 450 ° C. Ces normes CMOS, combinées à la différence de paramètre de maille entre l'InAs et le silicium, ont empêché l'intégration de nanofils InAs pour les dispositifs nanoélectroniques. Dans cette thèse, deux nouvelles préparations de surface du Si ont été étudiées impliquant des traitements Hydrogène in situ et conduisant à la croissance verticale et auto-catalysée de nanofils InAs compatible avec les limitations CMOS. Les différents mécanismes de croissance résultant de ces préparations de surface sont discutés en détail et un passage du mécanisme Vapor-Solid (VS) au mécanisme Vapor-Liquid-Solid (VLS) est rapporté. Les rapports d'aspect très élevé des nanofils d'InAs sont obtenus en condition VLS: jusqu'à 50 nm de diamètre et 3 microns de longueur.

D'autre part, le $Bi_{1-x}Sb_x$ est le premier isolant topologique 3D confirmé expérimentalement. Dans ces nouveaux matériaux, la présence d'états surfacique conducteurs, entourant le coeur isolant, peut héberger les fermions de Majorana utilisés comme Qubits. Cependant, la composition du $Bi_{1-x}Sb_x$ doit être comprise entre 0,08 et 0,24 pour que le matériau se comporte comme un isolant topologique. Nous rapportons pour la première fois la croissance de nanofils $Bi_{1-x}Sb_x$ sans défaut et à composition contrôlée sur Si. Différentes morphologies sont obtenues, y compris des nanofils, des nanorubans et des nanoflakes. Leur diamètre peut être de 20 nm pour plus de 10 microns de long, ce qui en fait des candidats idéaux pour des dispositifs quantiques. Le rôle clé du flux Bi, du flux de Sb et de la température de croissance sur la densité, la composition et la géométrie des structures à l'échelle nanométrique est étudié et discuté en détail.